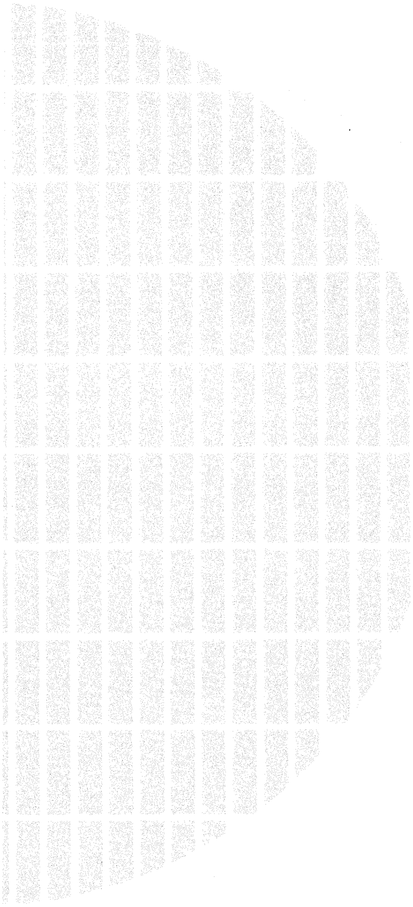
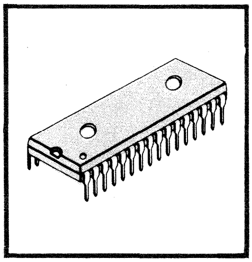
SAMSUNG

Data Book



MOS Memory

Vol. 3 1992/93



- EEPROM
- MASK ROM

PRINTED IN KOREA

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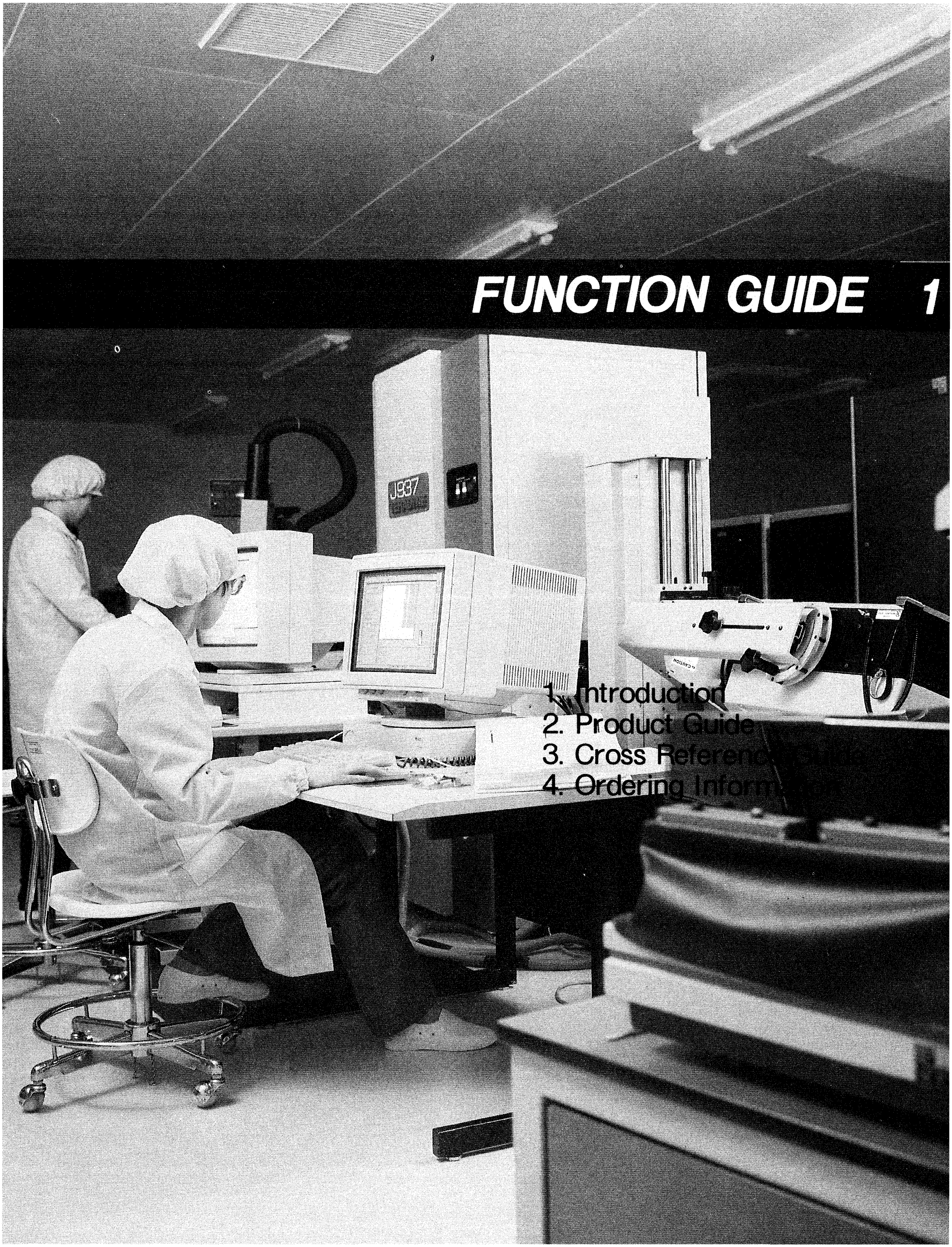
FUNCTION GUIDE 1



1. Introduction
2. Product Guide
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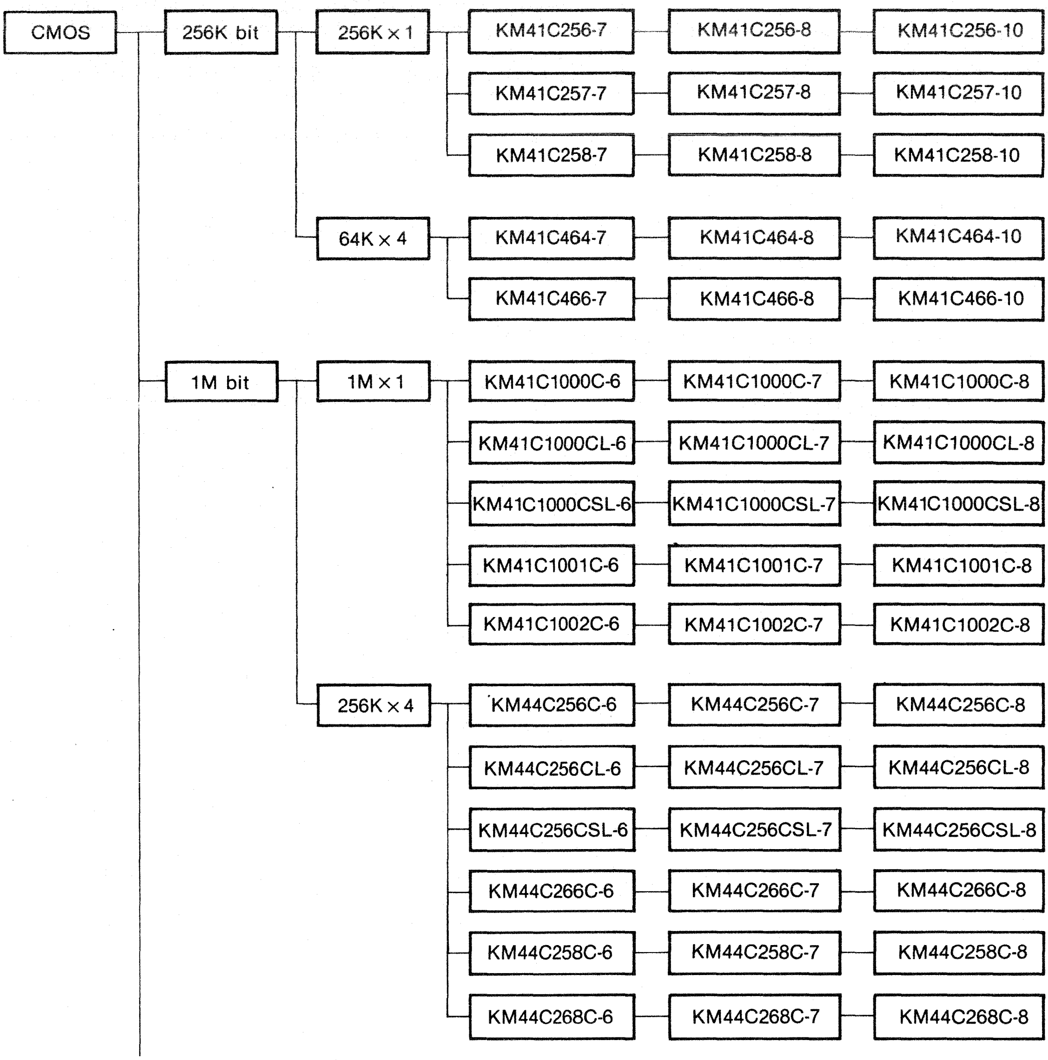
4. Ordering Information

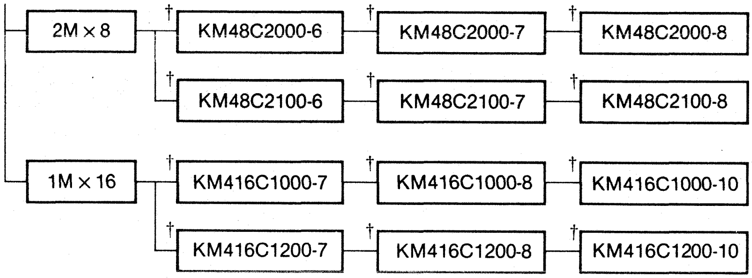
1. INTRODUCTION

1.1 Dynamic RAM



- 4M bit
  - 4M × 1
    - KM41C4000A-7 — KM41C4000A-8 — KM41C4000A-10
    - KM41C4000AL-7 — KM41C4000AL-8 — KM41C4000AL-10
    - KM41C4000ASL-7 — KM41C4000ASL-8 — KM41C4000ASL-10
    - KM41C4001A-7 — KM41C4001A-8 — KM41C4001A-10
    - KM41C4002A-7 — KM41C4002A-8 — KM41C4002A-10
    - *KM41C4000B-6 — *KM41C4000B-7 — *KM41C4000B-8
  - 1M × 4
    - KM44C1000A-7 — KM44C1000A-8 — KM44C1000A-10
    - KM44C1000AL-7 — KM44C1000AL-8 — KM44C1000AL-10
    - KM44C1000ASL-7 — KM44C1000ASL-8 — KM44C1000ASL-10
    - KM44C1002A-7 — KM44C1002A-8 — KM44C1002A-10
    - KM44C1010A-7 — KM44C1010A-8 — KM44C1010A-10
    - KM44C1012A-7 — KM44C1012A-8 — KM44C1012A-10
    - *KM44C1000B-6 — *KM44C1000B-7 — *KM44C1000B-8
  - 256K × 16
    - *KM416C256-7 — *KM416C256-8 — *KM416C256-10
    - *KM416C256L-7 — *KM416C256L-8 — *KM416C256L-10
    - *KM416C256SL-7 — *KM416C256SL-8 — *KM416C256SL-10
    - *KM416C256LL-7 — *KM416C256LL-8 — *KM416C256LL-10

CMOS	4M bit	256K × 18	*KM418C256-7	*KM418C256-8	*KM418C256-10
			*KM418C256L-7	*KM418C256L-8	*KM418C256L-10
			*KM418C256SL-7	*KM418C256SL-8	*KM418C256SL-10
			*KM418C256LL-7	*KM418C256LL-8	*KM418C256LL-10
		512K × 8	*KM48C512-7	*KM48C512-8	*KM48C512-10
			*KM48C512L-7	*KM48C512L-8	*KM48C512L-10
			*KM48C512SL-7	*KM48C512SL-8	*KM48C512SL-10
			*KM48C512LL-7	*KM48C512LL-8	*KM48C512LL-10
		512K × 9	*KM49C512-7	*KM49C512-8	*KM49C512-10
			*KM49C512L-7	*KM49C512L-8	*KM49C512L-10
			*KM49C512SL-7	*KM49C512SL-8	*KM49C512SL-10
			*KM49C512LL-7	*KM49C512LL-8	*KM49C512LL-10
	16M bit	16M × 1	*KM41C16000-6	*KM41C16000-7	*KM41C16000-8
			*KM41C16000L-6	*KM41C16000L-7	*KM41C16000L-8
			*KM41C16100-6	*KM41C16100-7	*KM41C16100-8
			*KM41C16100L-6	*KM41C16100L-7	*KM41C16100L-8
		4M × 4	*KM44C4000-6	*KM44C4000-7	*KM44C4000-8
			*KM44C4000L-6	*KM44C4000L-7	*KM44C4000L-8
			*KM44C4100-6	*KM44C4100-7	*KM44C4100-8
			*KM44C41000L-6	*KM44C41000L-7	*KM44C41000L-8



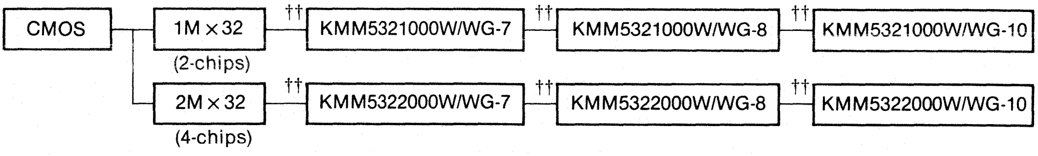
*: New Product
†: Preliminary Product
††: Under Development

1.2 Dynamic RAM Module

CMOS	256K × 8 (2-chips)	KMM58256CN-6	KMM58256CN-7	KMM58256CN-8
	256K × 9 (3-chips)	KMM59256CN-7	KMM59256CN-8	
	1M × 8	KMM581000C-6	KMM581000C-7	KMM581000C-8
	1M × 9	KMM591000C-6	KMM591000C-7	KMM591000C-8
	256K × 36	KMM536256C/CG-7	KMM536256C/CG-8	
	512K × 32	* KMM532512CV/CVG-6	* KMM532512CV/CVG-7	* KMM532512CV/CVG-8
	512K × 36	KMM536512C/CG-7	KMM536512C/CG-8	
	512K × 40	KMM540512C/CG/CM-6	KMM540512C/CG/CM-7	KMM540512C/CG/CM-8
	1M × 8 (2-chips)	KMM581000AN-7	KMM581000AN-8	KMM581000AN-10
		KMM581020AN-7	KMM581020AN-8	KMM581020AN-10
		* KMM581000BN-6	* KMM581000BN-7	* KMM581000BN-8
	1M × 9 (3-chips)	KMM591000AN-7	KMM591000AN-8	KMM591000AN-10
		KMM591020AN-7	KMM591020AN-8	KMM591020AN-10
		* KMM591000BN-6	* KMM591000BN-7	* KMM591000BN-8
	4M × 8	KMM584000A-7	KMM584000A-8	KMM584000A-10
		KMM584020A-7	KMM584020A-8	KMM584020A-10
		* KMM584000B-6	* KMM584000B-7	* KMM594000B-8

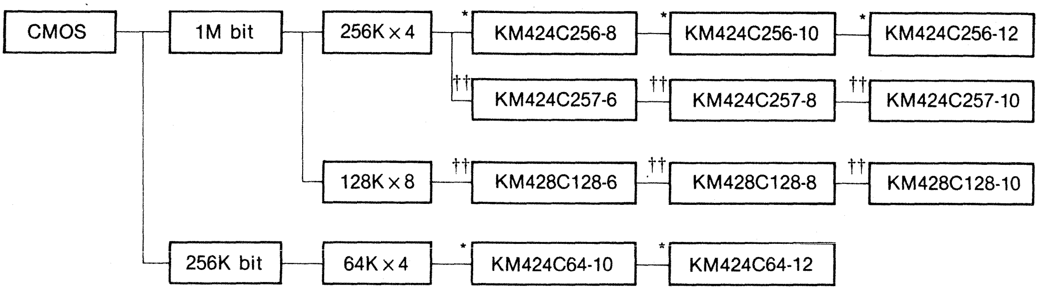
CMOS	4M × 9	KMM594000A-7	KMM594000A-8	KMM594000A-10
		KMM594020A-7	KMM594020A-8	KMM594020A-10
		*KMM594000B-6	*KMM594000B-7	*KMM594000B-8
	1M × 32	KMM5321000AV/AVG-7	KMM5321000AV/AVG-8	KMM5321000AV/AVG-10
		*KMM5321000BV/BVG-6	*KMM5321000BV/BVG-7	*KMM5321000BV/BVG-8
	1M × 36	KMM5361000A/AG-7	KMM5361000A/AG-8	KMM5361000A/AG-10
		*KMM5361000A1/A1G-7	*KMM5361000A1/A1G-8	*KMM5361000A1/A1G-10
		*KMM5361000B/BG-6	*KMM5361000B/BG-7	*KMM5361000B/BG-8
		*KMM5361000B1/B1G-6	*KMM5361000B1/B1G-7	*KMM5361000B1/B1G-8
	2M × 32	KMM5322000AV/AVG-7	KMM5322000AV/AVG-8	KMM5322000AV/AVG-10
		*KMM5322000BV/BVG-6	*KMM5322000BV/BVG-7	*KMM5322000BV/BVG-8
	2M × 36	KMM5362000A/AG-7	KMM5362000A/AG-8	KMM5362000A/AG-10
		*KMM5362000A1/A1G-7	*KMM5362000A1/A1G-8	*KMM5362000A1/A1G-10
		*KMM5362000B/BG-6	*KMM5362000B/BG-7	*KMM5362000B/BG-10
		*KMM5362000B1/B1G-6	*KMM5362000B1/B1G-7	*KMM5362000B1/B1G-10
	1M × 40	KMM5401000A/AG-7	KMM5401000A/AG-8	KMM5401000A/AG-10
		*KMM5401000B/BG-6	*KMM5401000B/BG-7	*KMM5401000B/BG-8
	2M × 40	KMM5402000A/AG-7	KMM5402000A/AG-8	KMM5402000A/AG-10
		*KMM5402000B/BG-6	*KMM5402000B/BG-7	*KMM5402000B/BG-8

CMOS	256K × 36 (2-chips)	*KMM536256W/WG-7	*KMM536256W/WG-8	*KMM536256W/WG-10
	512K × 32 (4-chips)	*KMM532512W3/W3G-7	*KMM532512W3/W3G-8	*KMM532512W3/W3G-10
	512K × 36 (4-chips)	*KMM536512W3/W3G-7	*KMM536512W3/W3G-8	*KMM536512W3/W3G-10
	4M × 8	*KMM584100N-6	*KMM584100N-7	*KMM584100N-8
	4M × 9 (3-chips)	*KMM594100N-6	*KMM594100N-7	KMM594100N-8
	16M × 8	*KMM5816000/T-6	*KMM5816000/T-7	*KMM5816000/T-8
		*KMM5816100/T-6	*KMM5816100/T-7	*KMM5816100/T-8
	16M × 9	*KMM5916000/T-6	*KMM5916000/T-7	*KMM5916000/T-8
		*KMM5916100/T-6	*KMM5916100/T-7	*KMM5916100/T-8
	4M × 32	*KMM5324100V/VG/VP-6	*KMM5324100V/VG/VP-7	*KMM5324100V/VG/VP-8
	4M × 36	*KMM5364100/G-6	*KMM5364100/G-7	KMM5364100/G-8
		*KMM5364000H/HG-6	*KMM5364000H/HG-7	*KMM5364000H/HG-8
		*KMM5364100H/HG-6	*KMM5364100H/HG-7	*KMM5364100H/HG-8
	8M × 32	*KMM5328100V/VG/VP-6	*KMM5328100V/VG/VP-7	*KMM5328100V/VG/VP-8
	8M × 36	KMM5368100/G-6	KMM5368100/G-7	KMM5368100/G-8
		*KMM5368000H/HG-6	*KMM5368000H/HG-7	*KMM5368000H/HG-8
		*KMM5368100H/HG-6	*KMM5368100H/HG-7	*KMM5368100H/HG-8
	4M × 40	*KMM5404000/G-6	*KMM5404000/G-7	*KMM5404000/G-8
		*KMM5404100/G-6	*KMM5404100/G-7	*KMM5404100/G-8



* New Product
†† Under Development

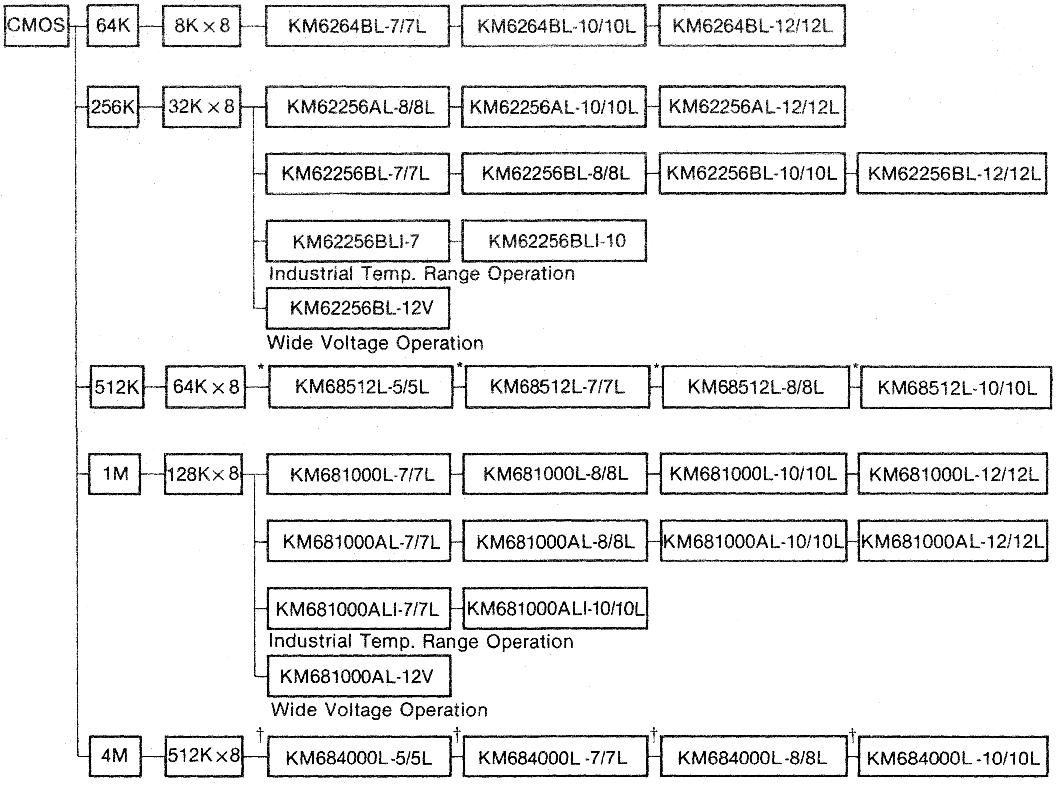
1.3 Video RAM



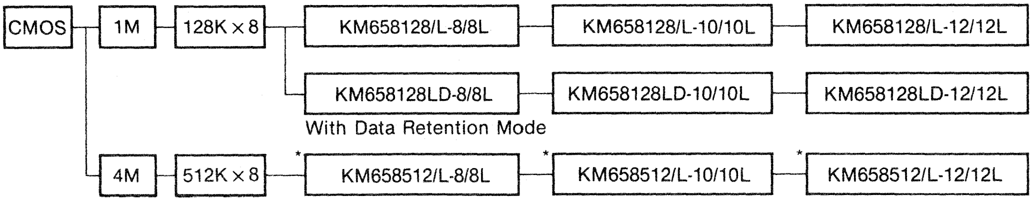
*: New Product
†: Preliminary Product
††: Under Development

1.4 Static RAM

Low Power SRAMs

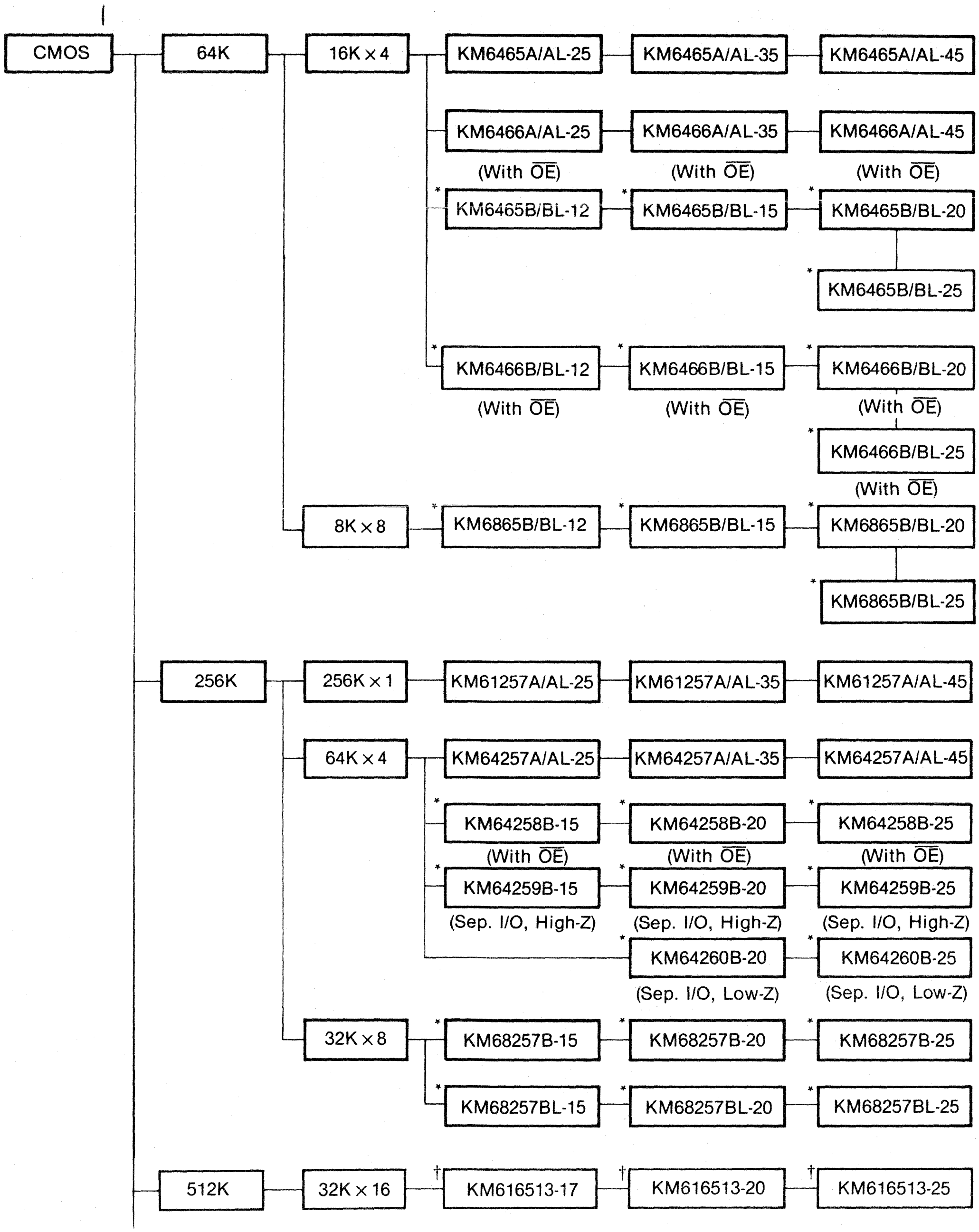


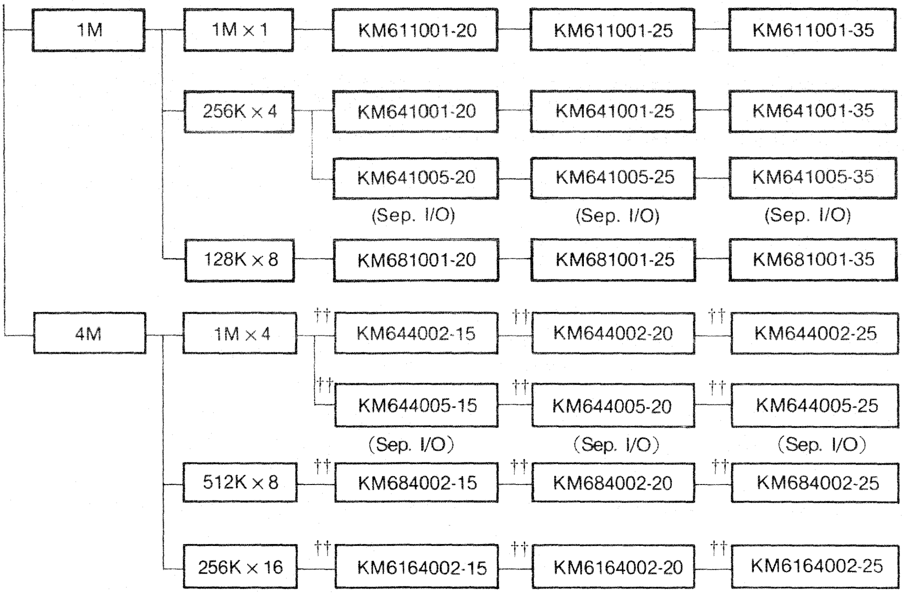
Pseudo SRAM Product Tree



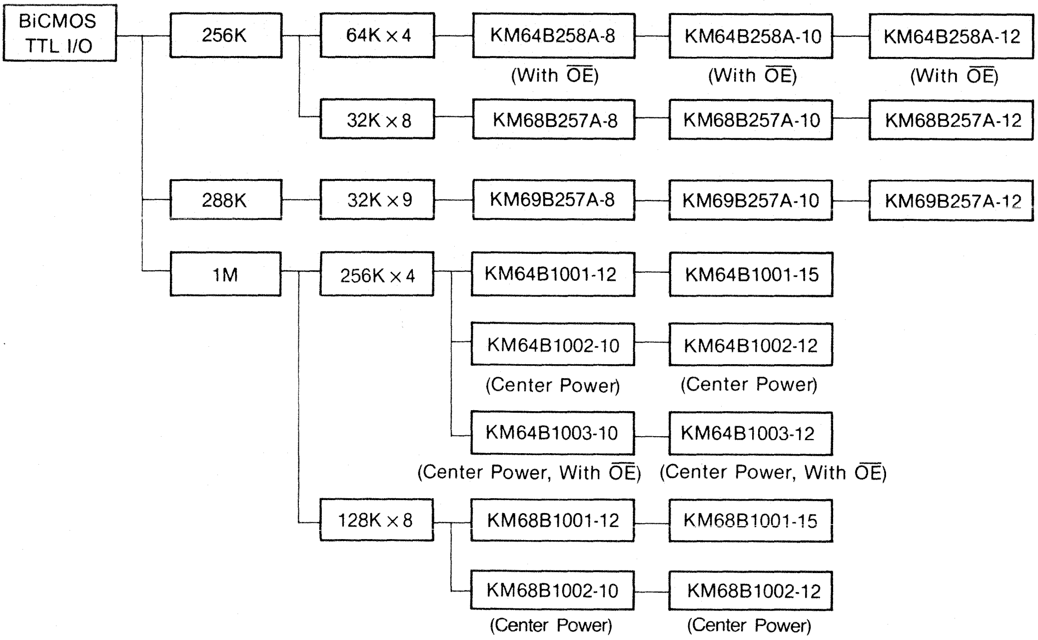
* New Product
† Preliminary Product
†† Under Development

High Speed SRAM

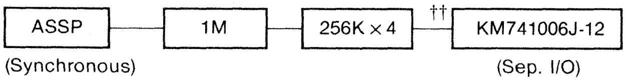



1M
1M × 1
KM611001-20
KM611001-25
KM611001-35
256K × 4
KM641001-20
KM641001-25
KM641001-35
KM641005-20
KM641005-25
KM641005-35
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
128K × 8
KM681001-20
KM681001-25
KM681001-35
4M
1M × 4
††
KM644002-15
††
KM644002-20
††
KM644002-25
††
KM644005-15
††
KM644005-20
††
KM644005-25
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
512K × 8
††
KM684002-15
††
KM684002-20
††
KM684002-25
256K × 16
††
KM6164002-15
††
KM6164002-20
††
KM6164002-25

* BiCMOS SRAM

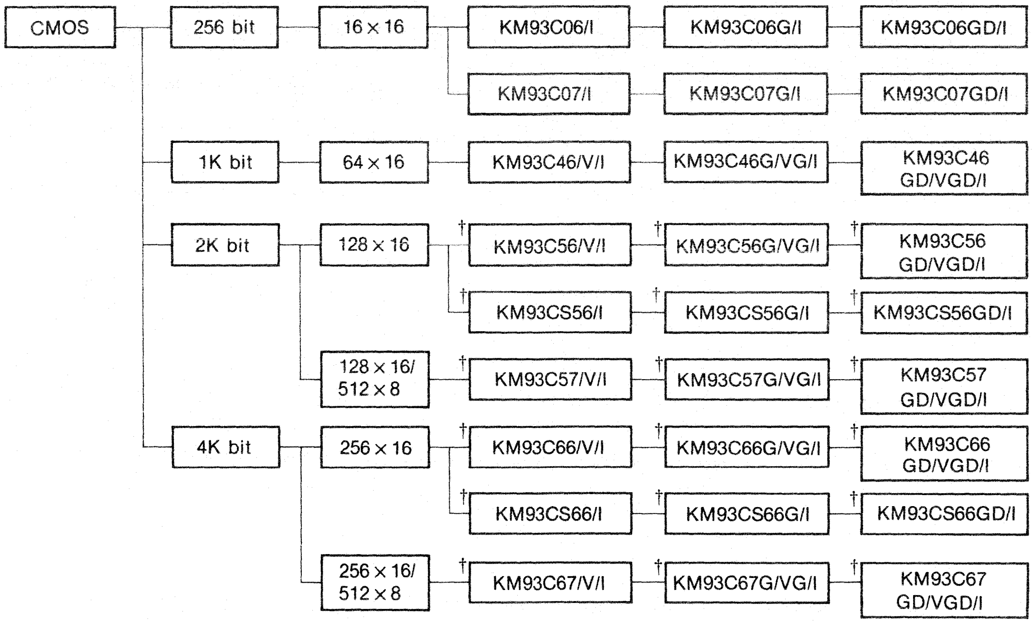


Specialty SRAM

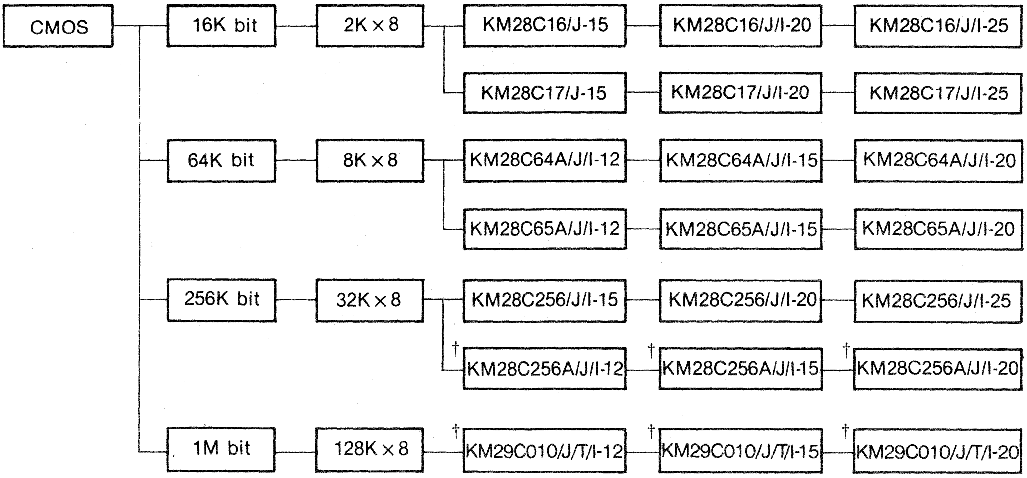


* New Product
† Preliminary Product
†† Under Development

1.5 Serial EEPROM



Parallel EEPROM



* New Product † Preliminary Product

1.6 MASKROM- I (Low Density)

CMOS	256K bit	32K × 8	KM23C256(G)-12	KM23C256(G)-15	KM23C256(G)-20
	512K bit	64K × 8	KM23C512(G)-12	KM23C512(G)-15	KM23C512(G)-20
	1M bit	128K × 8	KM23C1000-12	KM23C1000-15	KM23C1000-20
			KM23C1001-12	KM23C1001-15	KM23C1001-20
			KM23C1010(G)-12	KM23C1010(G)-15	KM23C1010(G)-20
			* KM23C1010J-12	* KM23C1010J-15	* KM23C1010J-20
			KM23C1011(G)-12	KM23C1011(G)-15	KM23C1011(G)-20
	2M bit	256K × 8	KM23C2000(G)-15	KM23C2000(G)-20	KM23C2000(G)-25
			† KM23C2000H(G)-10	† KM23C2000H(G)-12	† KM23C2000H(G)-15
			KM23C2001-15	KM23C2001-20	KM23C2001-25
			† KM23C2001H-10	† KM23C2001H-12	† KM23C2001H-15
		256K × 8/ 128K × 16	KM23C2100(FP)-15	KM23C2100(FP)-20	KM23C2100(FP)-25
			† KM23C2100H(FP)-10	† KM23C2100H(FP)-12	† KM23C2100H(FP)-15
	4M bit	512K × 8	KM23C4000A(G)-15	KM23C4000A(G)-20	KM23C4000A(G)-25
			* KM23C4000B(G)-12	* KM23C4000B(G)-15	* KM23C4000B(G)-20
			KM23C4000H(G)-10	KM23C4000H(G)-12	KM23C4000H(G)-15
			KM23C4001A(G)-15	KM23C4001A(G)-20	KM23C4001A(G)-25
			* KM23C4001B(G)-12	* KM23C4001B(G)-15	* KM23C4001B(G)-20
			KM23C4001H(G)-10	KM23C4001H(G)-12	KM23C4001H(G)-15
		512K × 8/ 256K × 16	* KM23C4100BG-12	* KM23C4100BG-15	* KM23C4100BG-20 ※
			KM23C4100A(FP)-15	KM23C4100A(FP)-20	KM23C4100A(FP)-25
			* KM23C4100B(FP)-12	* KM23C4100B(FP)-15	* KM23C4100B(FP)-20
			KM23C4100H(FP)-10	KM23C4100H(FP)-12	KM23C4100H(FP)-15
			KM23C4200B-12	KM23C4200B-15	KM23C4200B-20 ※

* New Product † Under Development

※ Both A and B ver. are available in 3Q '92

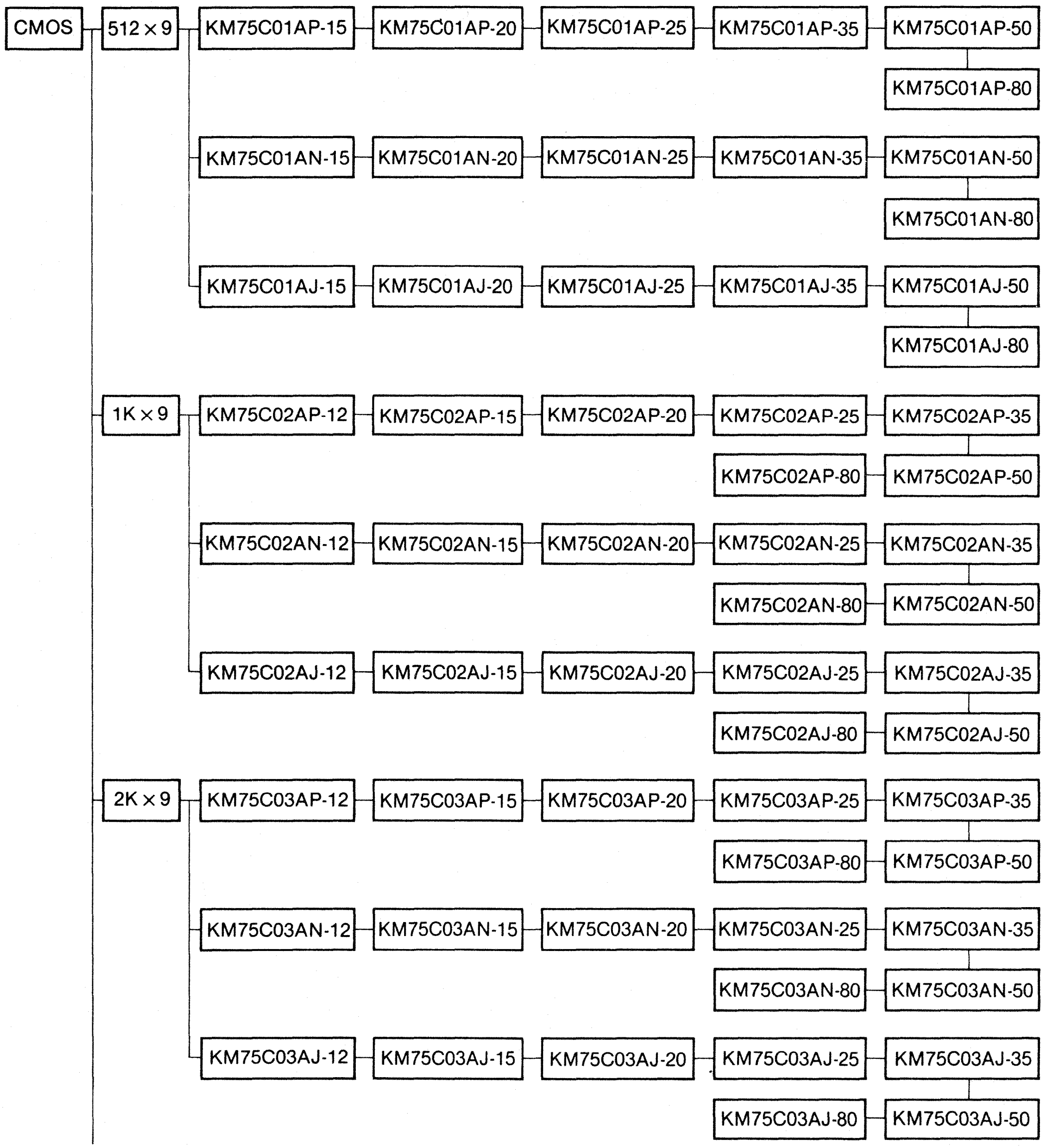
MASKROM-II (High Density)

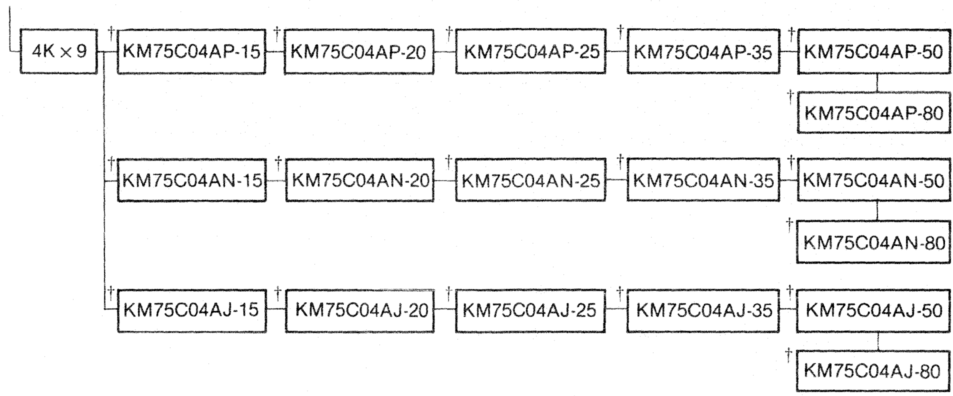
CMOS	8M bit	1M × 8	KM23C8000A(G)-15	KM23C8000A(G)-20	KM23C8000A(G)-25
			† KM23C8000H(G)-10	† KM23C8000H(G)-12	† KM23C8000H(G)-15
			KM23C8001A-15	KM23C8001A-20	KM23C8001A-25
			† KM23C8001H-10	† KM23C8001H-12	† KM23C8001H-15
		1M × 8/ 512K × 16	KM23C8100A(G)-15	KM23C8100A(G)-20	KM23C8100A(G)-25
			KM23C8100AFP1-15	KM23C8100AFP1-20	KM23C8100AFP1-25
			KM23C8100AFP2-15	KM23C8100AFP2-20	KM23C8100AFP2-25
			† KM23C8100H(G)-10	† KM23C8100H(G)-12	† KM23C8100H(G)-15
			† KM23C8100HFP1-10	† KM23C8100HFP1-12	† KM23C8100HFP1-15
			† KM23C8100HFP2-10	† KM23C8100HFP2-12	† KM23C8100HFP2-15
	16M bit	2M × 8/ 1M × 16	KM23C16000(G)-15	KM23C16000(G)-20	KM23C16000(G)-25
			* KM23C16000FP-15	* KM23C16000FP-20	* KM23C16000FP-25
			† KM23C16100(G)-15	† KM23C16100(G)-20	† KM23C16100(G)-25
			† KM23C16100FP-15	† KM23C16100FP-20	† KM23C16100FP-25
	32M bit	4M × 8/ 2M × 16	† KM23C32000-15	† KM23C32000-20	† KM23C32000-25
			† KM23C32000G-15	† KM23C32000G-20	† KM23C32000G-25
			† KM23C32000FP-15	† KM23C32000FP-20	† KM23C32000FP-25
			† KM23C32100-15	† KM23C32100-20	† KM23C32100-25
			† KM23C32100G-15	† KM23C32100G-20	† KM23C32100G-25
			† KM23C32100FP-15	† KM23C32100FP-20	† KM23C32100FP-25

* New Product
† Under Development

1.7 Application Specific Memory

STANDARD FIFO





*AP: PDIP (0.6")
AN: PDIP (0.3")
AJ: PLCC
†: Preliminary Product

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM41C256P	256K x 1	70/80/100	CMOS	Fast Page	16 Pin DIP	Now
	KM41C256J	256K x 1	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C256Z	256K x 1	70/80/100	CMOS	Fast Page	16 Pin ZIP	Now
	KM41C257P	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin DIP	Now
	KM41C257J	256K x 1	70/80/100	CMOS	Nibble Mode	18 Pin PLCC	Now
	KM41C257Z	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin ZIP	Now
	KM41C258P	256K x 1	70/80/100	CMOS	Static Column	16 Pin DIP	Now
	KM41C258J	256K x 1	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C258Z	256K x 1	70/80/100	CMOS	Static Column	16 Pin ZIP	Now
	KM41C464P	64K x 4	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C464J	64K x 4	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C464Z	64K x 4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C466P	64K x 4	70/80/100	CMOS	Static Column	18 Pin DIP	Now
	KM41C466J	64K x 4	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C466Z	64K x 4	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
1M bit	KM41C1000CP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CSLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CSLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CSLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CSLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CSLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CSLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CSLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1001CP	1M x 1	60/70/80	CMOS	Nibble Mode	18 Pin DIP	Now
	KM41C1001CJ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin SOJ	Now
	KM41C1001CZ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin ZIP	Now
	KM41C1001CV	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Forward)	Now
	KM41C1001CVR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Reverse)	Now
	KM41C1001CT	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Forward)	Now
	KM41C1001CTR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Reverse)	Now
	KM41C1002CP	1M x 1	60/70/80	CMOS	Static Column	18 Pin DIP	Now
	KM41C1002CJ	1M x 1	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM41C1002CZ	1M x 1	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM41C1002CV	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM41C1002CVR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM41C1002CT	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM41C1002CTR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
1M bit	KM44C256CP	256K × 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CJ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CZ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CV	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CVR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CT	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CTR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CLP	256K × 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CLJ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CLZ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CLV	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CLVR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CLT	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CLTR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CSLP	256K × 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CSLJ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CSLZ	256K × 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CSLV	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CSLVR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CSLT	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CSLTR	256K × 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C266CP	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C266CJ	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C266CZ	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C266CV	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C266CVR	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C266CT	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C266CTR	256K × 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C258CP	256K × 4	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM44C258CJ	256K × 4	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM44C258CZ	256K × 4	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM44C258CV	256K × 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM44C258CVR	256K × 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM44C258CT	256K × 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM44C258CTR	256K × 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C268CP	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C268CJ	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C268CZ	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin ZIP	Now
	KM44C268CV	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C268CVR	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C268CT	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C268CTR	256K × 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Reverse)	Now
4M bit	*KM41C4000BP	4M × 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BJ	4M × 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BZ	4M × 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BV	4M × 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BVR	4M × 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BT	4M × 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BTR	4M × 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BLP	4M × 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M bit	*KM41C4000BLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BSLP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BSLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BSLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BSLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BSLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BSLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BSLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
4M B/W	*KM48C512J	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512Z	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512T	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512TR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512SLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512SLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512SLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512SLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512J	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512Z	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512T	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512TR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512SLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512SLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512SLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512SLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM416C256J	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256Z	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256SLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256SLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M B/W	*KM418C256J	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256Z	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256SLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256SLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
16M	*KM41C16000J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
16M B/W	†KM48C2000J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM48C2100J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM416C1000J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92
	†KM416C1200J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92

*: New Product †: Preliminary Product

2.2 Dynamic RAM Module

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
1M DRAM Base	KMM58256CN	256K×8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM59256CN	256K×9	70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581000C	1M×8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM591000C	1M×9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM536256C/CG	256K×36	70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	KMM532512CV/CVG	512K×32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM536512C/CG	512K×36	70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM540512C/CG/CM	512K×40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
4M DRAM Base	KMM581000AN	1M×8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581020AN	1M×8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM581000BN	1M×8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM591000AN	1M×9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM591020AN	1M×9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM591000BN	1M×9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM584000A	4M×8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM584020A	4M×8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM584000B	4M×8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM594000A	4M×9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM594020A	4M×9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM594000B	4M×9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM5321000AV/AVG	1M×32	70/80/100	Fast Page	S, 72 Pin SIMM	0.855	Now
	*KMM5321000BV/BVG	1M×32	60/70/80	Fast Page	S, 72 Pin SIMM	0.855	Now
	KMM5361000A/AG	1M×36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM5361000A1/A1G	1M×36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5361000B/BG	1M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	*KMM5361000B1/B1G	1M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5322000AV/AVG	2M×32	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5322000BV/BVG	2M×32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5362000A/AG	2M×36	70/80/100	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5362000A1/A1G	2M×36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5362000B/BG	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	'92. 3Q
	*KMM5362000B1/B1G	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5401000A/AG/AM	1M×40	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5401000B/BG/BM	1M×40	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5402000A/AG/AM	2M×40	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5402000B/BG/BM	2M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q

2.2 Dynamic RAM Module (Continued)

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
4M B/W Wide DRAM Base	*KMM536256W/WG	256K×36	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	Now
	*KMM532512W3/W3G	512K×32	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM536512W3/W3G	512K×36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
16M DRAM Base	*KMM584100N	4M×8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM594100N	4M×9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM5816000/T	16M×8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5816100/T	16M×8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916000/T	16M×9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916100/T	16M×9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5324100V/VG/VP	4M×32	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5364100/G	4M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5364000H/HG	4M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5364100H/HG	4M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5328100V/VG/VP	8M×32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5368100/G	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.375	Now
	*KMM5368000H/HG	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5368100H/HG	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5404000/G	4M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5404100/G	4M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
16M B/W Wide DRAM Base	††KMM5321000W/WG	1M×32	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	'92. 4Q
	††KMM5322000W/WG	2M×32	70/80/100	Fast Page	D, 72 Pin SIMM	0.8	'92. 4Q

Note: S: Single Side, D: Double Side
*: New Product, ††: Under Development

2.3 Video RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
1M bit	KM424C256J	256K×4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin SOJ	Now
	KM424C256Z	256K×4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin ZIP	Now
	††KM424C257J	256K×4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin SOJ 44 Pin TSOP II	3Q, '92
	††KM424C257Z	256K×4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin ZIP	3Q, '92
	††KM428C128Z	128K×8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin ZIP 44 Pin TSOP II	4Q, '91
	††KM428C128J	128K×8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin SOJ	4Q, '91
256K bit	KM424C64P	64K×4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin DIP	Now
	KM424C64Z	64K×4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin ZIP	Now

2.4 Static RAM

Slow SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation			Package	Remark
					Active(max.) TTL. DC	Active(max.) TTL. Min	Standby(max.) CMOS		
64K	KM6264BL	8K×8	70/100/120	CMOS	15mA	55mA	100μA	DIP/SDIP/SOP	Now
	KM6264BL-L	8K×8	70/100/120	CMOS	15mA	55mA	10μA	DIP/SDIP/SOP	Now
256K	KM62256AL	32K×8	80/100/120	CMOS	45mA	70mA	100μA	DIP/SOP	Now
	KM62256AL-L	32K×8	80/100/120	CMOS	45mA	70mA	50μA	DIP/SOP	Now
	KM62256BL	32K×8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SDIP/SOP	Now
	KM62256BL-L	32K×8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SDIP/SOP	Now
	*KM62256BLI	32K×8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM62256BL-V	32K×8	240	CMOS	15mA	70mA	50μA	DIP/SDIP/SOP	Now
512K	*KM68512L	64K×8	55/70/85/100	CMOS	15mA	70mA	100μA	SOP/TSOP	3Q.'92
	*KM68512L-L	64K×8	55/70/85/100	CMOS	15mA	70mA	20μA	SOP/TSOP	3Q.'92
1M	KM681000L	128K×8	70/85/100/120	CMOS	25mA	70mA	100μA	DIP/SOP	Now
	KM681000L-L	128K×8	70/85/100/120	CMOS	25mA	70mA	20μA	DIP/SOP	Now
	*KM681000AL	128K×8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SOP/TSOP	Now
	*KM681000AL-L	128K×8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SOP/TOP	Now
	*KM681000ALI	128K×8	70/100	CMOS	20mA	70mA	100μA	DIP/SOP	Now
	*KM681000ALI-L	128K×8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM681000AL-V	128K×8	240	CMOS	15mA	70mA	50μA	DIP/SOP/TSOP	Now
4M	†KM684000L	512K×8	55/70/85/100	CMOS	25mA	70A	100μA	DIP/SOP/TSOP	3Q.'92
	†KM684000L-L	512K×8	55/70/85/100	CMOS	25mA	70mA	20μA	DIP/SOP/TSOP	3Q.'92

*: New Product †: Preliminary ††: Under Development

Pseudo SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation		Package	Remark
					Active(max.) TTL. Min	Standby(max.) CMOS		
1M	KM658128	128K×8	80/100/120	CMOS	70mA	2mA	DIP/SDIP/SOP	Now
	KM658128L	128K×8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128L-L	128K×8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
	KM658128LD	128K×8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128LD-L	128K×8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
4M	*KM658512	512K×8	80/100/120	CMOS	75mA	1mA	DIP/SOP/TSOP	3Q.'92
	*KM658128L	512K×8	80/100/120	CMOS	75mA	200μA	DIP/SOP/TSOP	3Q.'92
	*KM658128L-L	512K×8	80/100/120	CMOS	75mA	100μA	DIP/SOP/TSOP	3Q.'92

*: New Product †: Preliminary ††: Under Development

High Speed & Ultra High Speed SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
64K	KM6465A	16K × 4	25/35/45	CMOS	100	2	22SDIP	Now
	KM6465AL	16K × 4	25/35/45	CMOS	100	0.1	22SDIP	Now
	*KM6465B	16K × 4	12/15/20/25	CMOS	140	1	22SDIP	Now
	KM6465BL	16K × 4	12/15/20/25	CMOS	140	0.1	22DIP	Now
	KM6466A	16K × 4	25/35/45	CMOS	120	2	22SDIP/SOJ	Now
	KM6466AL	16K × 4	25/35/45	CMOS	120	0.1	22SDIP/SOJ	Now
	*KM6466B	16K × 4	12/15/20/25	CMOS	140	1	24SDIP/SOJ	Now
	KM6466BL	16K × 4	12/15/20/25	CMOS	140	0.1	24DIP/SOJ	Now
	*KM6865B	8K × 8	12/15/20/25	CMOS	140	1	28SDIP/SOJ	Now
	KM6865BL	8K × 8	12/15/20/25	CMOS	140	0.1	28DIP/SOJ	Now
256K	KM61257A	256K × 1	25/35/45	CMOS	100	2	24SDIP/SOJ	Now
	KM61257AL	256K × 1	25/35/45	CMOS	100	0.1	24SDIP/SOJ	Now
	KM64257A	64K × 4	25/35/45	CMOS	100	2	24SDIP/SOJ	Now
	KM64257AL	64K × 4	25/35/45	CMOS	100	0.1	24SDIP/SOJ	Now
	†KM64258B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	†KM64B258A	64K × 4	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
	*KM64259B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM64260B	64K × 4	20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM68257B	32K × 8	15/20/25	CMOS	150	2	28SDIP/SOJ	Now
	*KM68257BL	32K × 8	15/20/25	CMOS	130	0.1	28SDIP/SOJ	Now
	†KM68B257A	32K × 8	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
	KM69B257A	32K × 9	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
1M	*KM611001	1M × 1	20/25/35	CMOS	140	2	28SDIP/SOJ	Now
	*KM641001	256K × 4	20/25/35	CMOS	150	2	28SDIP/SOJ	Now
	*KM641005	256K × 4	20/25/35	CMOS	150	2	32SDIP/SOJ	Now
	†KM64B1001	256K × 4	12/15	BiCMOS	170	20	28SDIP/SOJ	3Q '92
	KM64B1002	256K × 4	10/12	BiCMOS	160	20	28SOJ	4Q '92
	KM64B1003	256K × 4	10/12	BiCMOS	160	20	28SOJ	4Q '92
	*KM681001	128K × 8	20/25/35	CMOS	160	2	32SDIP/SOJ	Now
	†KM68B1001	128K × 8	12/15	BiCMOS	180	20	32SDIP/SOJ	3Q '92
	KM68B1002	512K × 8	10/12	BiCMOS	180	20	28SOJ	4Q '92

Synchronous SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	KM741006	256K × 4	12	CMOS	190	80	36SOJ	4Q '92

Synchronous

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	††KM741006 ††KM781006 ††KM791006	256K × 4 128K × 8 128K × 9	10/12 10/12 10/12	CMOS CMOS CMOS	170 170 170	3 3 3	32SOJ 36SOJ 36SOJ	4Q '92 4Q '92 4Q '92

*: New Product †: Preliminary Product ††: Under Development

2.5 EEPROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remarks
256 bit	KM93C06/G/GD/I	16 × 16	1MHz	CMOS	Ext.-timed	8DIP/8SOP	Now
	KM93C07/G/GD/I	16 × 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
1K bit	KM93C46/G/GD/I	64 × 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64 × 16	250KHz	CMOS	3.0V Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128 × 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS56/G/GD/I	128 × 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C57/G/GD/I	256 × 8/128 × 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C56V/VG/VGD/I	128 × 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C57V/VG/VGD/I	256 × 8/128 × 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
4K bit	KM93C66/G/GD/I	256 × 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS66/G/GD/I	256 × 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C67/G/GD/I	512 × 8/128 × 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C66V/VG/VGD/1	256 × 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C67V/VG/VGD/I	512 × 8/128 × 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
16K bit	KM28C16/J	2K × 8	150/200/250	CMOS	32B Page Mode, D-P	24DIP/32PLCC	Now
	KM28C16I/JI	2K × 8	200/250	CMOS	Industrial	24DIP/32PLCC	Now
	KM28C17/J	2K × 8	150/200/250	CMOS	32B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C17I/JI	2K × 8	200/250	CMOS	Industrial	28DIP/32PLCC	Now
64K bit	KM28C64A/AJ	8K × 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K × 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K × 8	120/150/200	CMOS	64B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K × 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
256K bit	KM28C256/J	32K × 8	150/200/250	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C256I/JI	32K × 8	150/200/250	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C256A/AJ	32K × 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	4Q '92
	KM28C256AI/AJI	32K × 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	4Q '92
1M bit	KM29C010/J/T	128K × 8	120/150/200	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	4Q '92
	KM29C010I/JI	128K × 8	120/150/200	CMOS	Industrial	32TSOP	4Q '92

*: D-P: Data-Polling, R/B: Ready/Busy, T-B: Toggle Bit

2.6 Mask ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM23C256(G)	32K × 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
512K bit	KM23C512(G)	64K × 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
1M bit	KM23C1000	128K × 8	120/150/200	CMOS	Programmable CE	28DIP	Now
	KM23C1001	128K × 8	120/150/200	CMOS	Programmable OE	28DIP	Now
	KM23C1010(G)	128K × 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C1010J	128K × 8	120/150/200	CMOS	Programmable CE & OE	32PLCC	Now
	KM23C1011(G)	128K × 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
2M bit	KM23C2000(G)	256K × 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C2000H(G)	256K × 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C2001	256K × 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C2001H	256K × 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C2100(FP)	256K × 8/ 128K × 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C2100H(FP)	256K × 8/ 128K × 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	3Q '92
4M bit	KM23C4000A(G)	512K × 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C4000B(G)	512K × 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4000H(G)	512K × 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4001A(G)	512K × 8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4001B(G)	512K × 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C4001H(G)	512K × 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4100BG	512K × 8/ 256K × 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40SOP	Now
	KM23C4100A(FP)	512K × 8/ 256K × 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C4100B(FP)	512K × 8/ 256K × × 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	2Q '92
	KM23C4100H(FP)	512K × 8/ 256K × 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	KM23C4200B	512K × 8/ 256K × 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	Now

Mask ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
8M bit	KM23C8000A(G)	1M x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C8000H(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C8001A	1M x 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C8001H	1M x 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C8100A(G)	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	Now
	KM23C8100AFP1	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	Now
	KM23C8100AFP2	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C8100H(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	3Q '92
	†KM23C8100HFP1	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	3Q '92
	†KM23C8100HFP2	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
16M bit	KM23C16000(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	Now
	*KM23C16000FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C16100(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	3Q '92
	†KM23C16100FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
32M bit	†KM23C32000	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32000G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32000FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92
	†KM23C32100	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32100G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32100FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92

*: New Product †: Under Development

2.7 FIFO

Capacity	Part Number	Organization	Speed	Technology	Features	Package	Remark
Standard FIFO	KM75C01AP	512×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C01AN	512×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C01AJ	512×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C02AP	1K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C02AN	1K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C02AJ	1K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C03AP	2K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C03AN	2K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C03AJ	2K×9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C04AP	4K×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	4Q '92
	KM75C04AN	4K×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	4Q '92
	KM75C04AJ	4K×9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	4Q '92

*: New Product
†: Preliminary Product

3. CROSS REFERENCE GUIDE

3.1 DRAM

Density	Org.	Mode	Samsung	Toshiba	Hitachi	Fujitsu	NEC	Oki
256K	×1	F. Page	KM41C256	TC51256	HM51256	MB81256	μPD41256	MSM51C256
		Nibble	KM41C257	TC51257	—	MB81257	—	MSM41257
		S. Column	KM41C258	TC51258	HM51258	MB81258	—	—
	×4	F. Page	KM41C464	TC51464	HM50464	MB81464	μPD41464	MSM41464
		S. Column	KM41C466	TC51466	—	MB81466	—	—
1M	×1	F. Page	KM41C1000	TC511000	HM511000	MB81C1000	μP0421000	MSM511000
		Nibble	KM41C1001	TC511001	HM511001	MB81C1001	μP0421001	MSM511001
		S. Column	KM41C1002	TC511002	HM511002	MB81C1002	μP0421002	MSM511002
	×4	F. Page	KM44C256	TC514256	HM514256	MB81C4256	μP0424256	MSM514256
		S. Column	KM44C258	TC514258	HM514258	MB81C4258	μP0424258	MSM514258
4M	×1	F. Page	KM41C4000	TC514100	HM514100	MB814100	μPD424100	MSM514100
		Nibble	KM41C4001	TC514101	HM514101	MB814101	μPD424101	MSM514101
		S. Column	KM41C4002	TC514102	HM514102	MB814102	μPD424102	MSM514102
	×4	F. Page	KM44C1000	TC514400	HM514400	MB814400	μPD424400	MSM514400
		S. Column	KM44C1002	TC514402	HM514402	MB814402	μPD424402	MSM514402
	×8	F. Page	KM48C512	TC514800A	HM514800	MB814800A	μPD424800	—
	×9	F. Page	KM49C512	TC514900A	HM514900	—	μPD424900	—
	×16	F. Page	KM416C256	TC514170B	HM514170	MB814170A	μPD424170	—
	×18	F. Page	KM418C256	TC514280B	HM514280	—	μPD424280	—
16M	×1	F. Page	KM41C16000	TC5116100	HM5116100	MB8116100	μPD4216100	—
	×4	F. Page	KM44C4000	TC5116400	HM5116400	MB8116400	μPD4216400	—

3.2 DYNAMIC RAM MODULE

Density	Organization	Samsung	Toshiba	Hitachi	NEC
2M bit	256K × 8(2C)	KMM58256CN	THM82500	HB56025608	—
2.3M bit	256K × 9(3C)	KMM59256CN	THM92500	HB56025609	—
8M bit	1M × 8	KMM581000	THM81000	HB56A18	MC-421000A8
9M bit	1M × 9	KMM591000	THM91000	HB56A19	MC-421000A9
8M bit	256K × 32	KMM532256	THM322500	HB56025632	—
9M bit	256K × 36	KMM536256	—	—	—
16M bit	512K × 32	KMM532512	THM325120	HB56051232	—
18M bit	512K × 36	KMM536512	—	HB56051236	—
20M bit	512K × 40	KMM540512	—	—	—
8M bit	1M × 8(2C)	KMM581000AN	—	HB56G18	—
9M bit	1M × 9(3C)	KMM591000AN	—	HB56G19	—
32M bit	4M × 8	KMM584000	THM84000	HB56A48	MC-424100A8
36M bit	4M × 9	KMM594000	THM94000	HB56A49	MC-424100A9
32M bit	1M × 32	KMM5321000	THM321000	HB56D132	—
36M bit	1M × 36	KMM5361000	THM5361020	HB56D136	MC-421000A36
64M bit	2M × 32	KMM5322000	THM322020	HB56D232	—
72M bit	2M × 36	KMM5362000	THM362020	HB56D236	MC-422000A36
40M bit	1M × 40	KMM5401000	THM401020	HB56A140	—
80M bit	2M × 40	KMM5402000	THM402020	—	—

3.3 VIDEO RAM

Density	Feature	Org.	Samsung	Toshiba	NEC	Hitachi	TI	Mitsubishi
256K	Minimum Feature	64K × 4	KM424C64		μPD41264 μPD42264	HM53461	TMS4461	M5M4C264
1M	Minimum Feature	256K × 4	KM424C256	TC524256 TC524256A/B	μPD42273	HM534251	TM544C250	
	Extended Feature	256K × 4	KM424C257	TC524258A/B TC524259B	μPD42274	HM534253 HM534252	TMS44C251	M5M442256
	Extended Feature	128K × 8	KM428C128	TC528126A/B TC528128A/B	μPD42275	HM538121 HM538122 HM538123	TMS48C121	M5M482128

3.4 Static RAM

Slow SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K × 8	KM6264BL/BL-L	HM6264AL/AL-L	CXK5864BL	TC5565AL	M5M5165	μPD4364L/L-L
256K	32K × 8	KM62256AL/AL-L KM62256BL/BL-L	HM62256L/L-L	CXK58257L/L-L	TC55257L	M5M5265	μPD43256AL
512K	64K × 8	KM68512L/L-L	—	—	—	—	—
1M	128K × 8	KM681000L/L-L KM681000AL/AL-L	HM628128L/L-L	CXK581000L CXK581001L	TC551001L	M5M51000	μPD431000L
4M	512K × 8	KM684000L/L-L	HM628512	CXK584000L	TC554001L	M5M5408	μPD434000

Pseudo SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	TOSHIBA	NEC	OKI	MOTOROLA
1M	128K × 8	KM658128/L/L-L	HM658128	TC518128A	μPD428128	MSM548128	MCM518128
4M	512K × 8	KM658512L/L-L	HM658512	TC518512	μPD428512	MSM548512	—

Fast SRAM

Density	Organization	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	Sony
64K	16K x 4	KM6465A/AL KM6465B/BL	HM6288/L	CY7C164 CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288	TC55416	CXK5464
	16K x 4 (With $\overline{OE}$)	KM6466A/AL KM6466B/BL	HM6289/L	CY7C166 CY7C166A	MB81C75	MT5C6405	IDT7189	MCM6290	TC55417	CXK5465
	8K x 8	KM6865B/BL		CY7C186A	MB81C78	MT5C6308	IDT7164	MCM6264	TC5588	CXK5863
256K	256K x 1	KM61257A/AL	HM6207H/L	CY7C197	MB81C81A	MT5C2561	IDT71257	MCM6207		CXK51256
	64K x 4	KM64257A/AL	HM6208H/L	CY7C194	MB81C84	MT5C2564	IDT71258	MCM6208	TC55464	CXK54256
	64K x 4 (With $\overline{OE}$)	KM64258B		CY7C196		MT5C2565	IDT61298	MCM6209	TC55465	
	64K x 4 (Sep. I/O, H-Z)	KM64259B		CY7C191	MB81C86		IDT71282			
	64K x 4 (Sep. I/O, L-Z)	KM64260B		CY7C192			IDT71281			
	32K x 8	KM68257B/BL	HM63832UH/L	CY7C199		MT5C2568	IDT71256	MCM6206	TC55328	CXK58258B
512K	32K x 16	KM616513							TC551632	
1M	1M x 1	KM611001	HM61100A/L	CY7C107		MT5C1001	IDT71027			
	256K x 4	KM641001	HM624256A/L	CY7C106		MT5C1005	IDT71028	MCM6229W		
	256K x 4 (Sep. I/O)	KM641005	HM624257A/L	CY7C101						CXK541000
	128K x 8	KM681001		CY7C108		MT5C1008	IDT71024	MCM6226W		CXK581020

BiCMOS SRAM

Density	Organization	Samsung	Hitachi	Cypress	Toshiba	Fijitsu	IDT	Motorola
256K	64K x 4(With OE)	KM64B258A	HM6709A	CY7B195	TC55B465		IDT61B298	MCM6709/A
	32K x 8	KM68B257A	HM628325H	CY7B199	TC55B328		IDT71B256	MCM6706/A
288K	32K x 9	KM69B257A			TC55B329			
1M	256K x 4	KM64B1001			TC55B4256	MB82B005	IDT71B028	
	256K x 4 (Center Power)	KM64B1002			TC55B4256			MCM6728
	256K x 4 (Center Power, with OE)	KM64B1003			TC55B4257			MCM6729
	128K x 8	KM68B1001			TC55B8128		IDT71B024	
	128K x 8 (Center Power)	KM68B1002			TC55B8128			MCM6726

3.5 EEPROM

Serial I/O EEPROM

Density	Samsung	N.S.	Exar	Micro Chip	SGSThomson	Catalyst	Rohm	AsahiKasai
256	KM93C06	NM9306		93C46	ST93C06			AK93C06
	KM93C07	NM9307		ER59256				
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AK93C46
	KM93CS46	NM93CS46			ST93C46		BR93CS46	
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56	XRM93C56A				BR93C56A	AK93C57
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93CS56	NM93CS56			ST93CS56			
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AK93C67
	KM93C67			93C66		CAT35C104		
	KM93CS66	NM93CS66			ST93CS66			
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

Parallel EEPROM

Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyst
16K	KM28C16	X2816B X2816C	DQ2816A DQ5516A	XL2816A	AT28C16		MSM28C16A	CAT28C16A
	KM28C17		DQ2817A DQ5517A	XL2817A	AT28C17			CAT28C17A
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
256K	KM28C256	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
	KM28C256A	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
1M	KM29C010				AT29C010			

3.6 Mask ROM Cross Reference Guide-1

Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	28 DIP	×8	KM23C256		HN623257P		LH23255D	M5M23256P	MB83256	
					HN623257PZ		LH53259D			
					HN623258P					
	32 SOP	×8	KM23C256G							
512K	28 DIP	×8	KM23C512			TC53512CP	LH23512D		MB83512	
							LH53514D			
							LH53515D			
	32 DIP	×8	KM23C512G							
1M	28 DIP	×8	KM23C1000	μPD23C1000A	HN62321P	TC531000CP	LH231000BD	M5M23C100	MB831000	
					HN62321BP		LH531000AD	M5M231000	MB831124	
					HN62331P					
			KM23C1001	μPD23C1010A	HN62321EP			M5M231001		
					HN62331EP					
	32 DIP	×8	KM23C1010	μPD23C1001E	HN62321AP	TC531001CP	LH231100BD			
				μPD23C1000EA	HN62331AP		LH530800D			
			KM23C1011				LH530900D			
	32 SOP	×8	KM23C1010G		HN62321AF	TC531001CF				
					HN62331AF					
			KM23C1011G							
2M	32 DIP	×8	KM23C2000	μPD23C2001			LH532300D		MB832000	CXK382001
							LH532100BD		MB832001	
			KM23C2001				LH532200BD			
							LH532400D			
	32 SOP	×8	KM23C2000G							
	40 DIP	×8/×16	KM23C2100	μPD23C2000	HN62412P		LH532000BD			
				μPD23C2000A	HN62422P		LH532500D			
	44 QFP	×8/×16	KM23C2100FP		HN62412FP					
					HN62422FP					

Mask ROM Cross Reference Guide—II

Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
4M	32 DIP	x8	KM23C4000A	µPD23C4001E	HN62304BP	TC534000P	LH534100BD	M5M23C401AP	MB834000A	CXK384001
					HN62314BP	TC534000AP				
					HN62324BP					
					HN62344BP					
			KM23C4001A				LH534200BD			
							LH534300D			
							LH534400D			
	32 SOP	x8	KM23C4000AG	µPD23C4001E	HN62304BF	TC534000F	LH534100BN	M5M23401AFP		
					HN62314BF	TC534000AF				
					HN62324BF					
					HN62344BF					
			KM23C4001HG				LH534200BN			
	40 DIP	X8/x16	KM23C4100A	µPD23C4000	HN62404P	TC534200P	LH534000BD	M5M23C400AP	MB834100A	
				µPD23C4000A	HN62414P		LH534500D		MB834200A	
					HN62424P					
					HN62444P					
	40 SOP	x8/x16	KM23C4100BG			TC534200F				
	44 QFP	x8/x16	KM23C4100AFP		HN62404FP				MB834200A	
					HN62414FP					
					HN62424FP					
					HN62444FP					
8M	32 DIP	x8	KM23C8000A	µPD23C8001E	HN62308BP		LH538100D	M5M23801P	MB838000	CXK388000
			KM23C8001A				LH538200D			
	32 SOP	x8	KM23C8000AG		HN62308BF			M5M23801FP		
	42 DIP	x8/x16	KM23C8100A	µPD23C8000	HN62408P	TC538200P	LH538000D	M5M23800P	MB838200	
	44 SOP	x8/x16	KM23C8100AG			TC538200F	LH538000N	M5M23800FP		
	44 QFP	x8/x16	KM23C8100AFP1		HN62408FP					
	64 QFP	x8/x16	KM23C8100AFP2				LH538000M		MB838200	
16M	42 DIP	x8/x16	KM23C16000	µPD23C16000	HN624016P	TC5316200P		M5M23160P	MB831620P	
					HN624017P					
			KM23C16100					M5M23168P		
	44 SOP	x8/x16	KM23C16000G		HN624017FB	TC5316200F		M5M23160FP	MB831620PF	
			KM23C16100G					M5M23168FP		
	64 QFP	x8/x16	KM23C16000FP				LH5316000M			
			KM23C16100FP							
32M	42 DIP	x16	KM23C32000							
	44 SOP	x8/x16	KM23C32000G				LH5332000N			
	64 QFP	x8/x16	KM23C32000FP				LH5332000M			

3.7 FIFO

Capacity	Org.	Samsung	AMD	IDT	Sharp	Cypress	TI
Standard FIFO	512 x 9	KM75C01A	Am7201	IDT7201SA/LA	LH5496/D	CY7C420(1)	74ACT7201A
	1K x 9	KM75C02A	Am7202	IDT7202SA/LA	LH5497/D	CY7C424(5)	74ACT7202
	2K x 9	KM75C03A	Am7203	IDT7203S/L	LH5498/DKM7	CY7C428(9)	
	4K x 9	KM75C04A	Am7204	IDT7204S/L	LH5499/D		

4. ORDERING INFORMATION

4.1 DRAM

KM 4 X X XXXXX X X X - XX

DRAM

ORGANIZATION

- 1: X1
- 4: X4
- 8: X8
- 9: X9
- 16: X16
- 18: X18

PROCESS & POWER

- C: CMOS, 5V
- V: CMOS, 3.3V

DENSITY

- 16000 (16M/4K, F.P)
- 16100 (16M/2K, F.P)
- 4000 (4M, 16M/4K, F.P)
- 4100 (16M/2K, F.P)
- 4001 (4M, N.B)
- 4002 (4M, S.C)
- 2000 (16M/4K, F.P)
- 2100 (16M/2K, F.P)
- 1000 (1M, 4M, 16M/4K, F.P)
- 1200 (16M/1K, F.P)
- 1001 (1M, 4M, N.B)
- 1002 (1M, 4M, S.C)
- 1010 (4M, F.P/WPB)
- 1012 (4M, S.C/WPB)
- 512 (4M, F.P)
- 256 (256K, 4M, F.P)
- 257 (256K, N.B)
- 258 (256K, 1M, S.C)
- 266 (1M, F.P/WPB)
- 268 (1M, S.C/WPB)
- 464 (256K, F.P)
- 466 (256K, S.C)

SPEED

- 6 : 60ns
- 7 : 70ns
- 8 : 80ns
- 10: 100ns

PACKAGE

- P: DIP
- J: SOJ
- Z: ZIP
- T: TSOP II (TR: Reverse)
- V: TSOP I (VR: Reverse)

POWER LIMITS

- BLANK: NORMAL
- L : LOW POWER
- SL : SUPER LOW POWER
- LL : SELF REFRESH

DIE REVISION

- BLANK: NONE
- A : FIRST REV.
- B : SECOND REV.
- C : THIRD REV.

4.2 DRAM MODULE

MODULE PART NUMBERING SYSTEM

KM M W WW XXXX Y Y Y Y Y Y —ZZ

MEMORY

MODULE

PIN/EDGE CONNECTOR

- •5: DRAM SIMM (EDGE CONNECTOR)
- •4: DRAM SIP (PINS)

ORGANIZATION

- •8 : X8 bits wide
- •9 : X9 bits wide
- •18 : X18 bits wide
- •32 : X32 bits wide
- •33 : X33 bits wide
- •36 : X36 bits wide
- •40 : X40 bits wide
- •144: X144 bits wide

DENSITY & MODE/FEATURE

16000: 16M F. Page, 4K refresh
16100: 16M F. Page, 2K refresh
8000: 8M F. Page, 4K refresh
8100: 8M F. Page, 2K refresh
4000: 4M F. Page, 1K/4K refresh
4001: 4M Nibble
4002: 4M S. Column
4020: 4M F. Page (Low Power)
4040: 4M F. Page (S. Low Power)
4100: 4M F. Page, 1K/2K refresh
1000: 1M F. Page
1001: 1M Nibble
1002: 1M S. Column
1010: 1M F. Page, L. Profile (.505″)
1020: 1M F. Page (Low Power)
1040: 1M F. Page (S. Low Power)
1005: 1M Slugger Module
512: 512K Page
514: 512K S. Column
532: 512K Page (Low Power)
256: 256K Page
258: 256K S. Column
276: 256K Page (Low Power)

SPEED

- •5 : 50ns
- •6 : 60ns
- •7 : 70ns
- •8 : 80ns
- •10: 100ns

LEAD FINISH/SPEC CUSTOMER

—STD. MODULE
- •BLANK: SOLDER
- •G : GOLD

—CUSTOMER
- •D: DEC
- •H: HP
- •M: IBM
- •P: APPLE
- •Q: COMPAQ

× 32 & × 33 ONLY PCB

- •V: ×32 & ×33 ONLY

NUMBER OF COMPONENTS

- •BLANK: MORE THAN 7 CHIPS
- •N : LESS THAN 8 CHIPS
- •W : BYTE-WORD WIDE BASE

PACKAGE (PCB) REVISION

- •BLANK: NONE
- •1 : FIRST REV.
- •2: SECOND REV.

PACKAGE (COMPONENT) TYPE

- •BLANK: SOJ OR PLCC
- •*T : TSOP

DIE (COMPONENT) REVISION

- •BLANK: NONE
- •A : FIRST REV.
- •B : SECOND REV.
- •C : THIRD REV.

4.3 SRAM ORDERING INFORMATION

KM XX X X XXXX X X X X — XX X X

MEMORY COMPONENT

DEVICE TYPE

- •6 : SRAM (Asyn.)
- •65: Pseudo SRAM
- •7 : SRAM (ASSP)

ORGANIZATIONS

- •1: ×1 bit
- •4: ×4 bits
- •2 or 8: ×8 bits
- •9: ×9 bits
- •16: x16 bits

TECHNOLOGY

- •BLANK: CMOS
- •B : BiCMOS (TTL I/O)

DENSITY & OPTIONS

- •64 : 64K Slow
- •65 : 64K Fast
- •66 : 64K Fast (with OE)
- •256 : 256K Slow
- •257 : 256K Fast
- •258 : 256K Fast (with OE)
- •259 : 256K Fast (Sep. I/O, High-Z)
- •260 : 256K Fast (Sep. I/O, Low-Z)
- •512 : 512K Slow
- •513 : 512K Fast
- •1000: 1M Slow
- •1001: 1M Fast
- •1002: 1M Fast (Center Power)
- •1003: 1M Fast (Center Power, with OE)
- •1005: 1M Fast (Sep. I/O)
- •1006: 1M Fast (Synch. Sep. I/O)
- •4000: 4M Slow
- •4002: 4M Fast (Center Power)
- •8128: 128K x 8 (1M PSRAM)
- •8512: 512K x 8 (4M PSRAM)

OPERATING V$_{CC}$

- •BLANK: 5V
- •V : 3V

POWER LIMITS

- •BLANK: High Power
- •L : Low Power
- •L-L : Low Low Power

SPEEDS

SLOW	FAST
•5 : 55ns	•8 : 8ns
•7 : 70ns	•10: 10ns
•8 : 80 or 85ns	•12: 12ns
•10: 100ns	•15: 15ns
•12: 120ns	•20: 20ns
	•25: 25ns
	•35: 35ns
	•45: 45ns

OPERATING TEMP.

- •BLANK: Commercial
- •I : Industrial

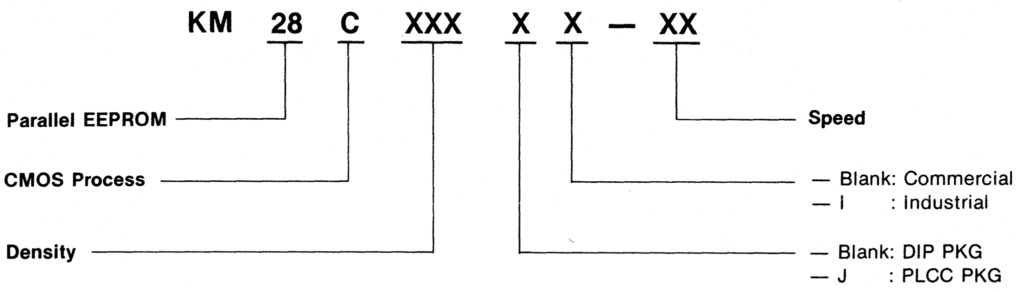
PACKAGES

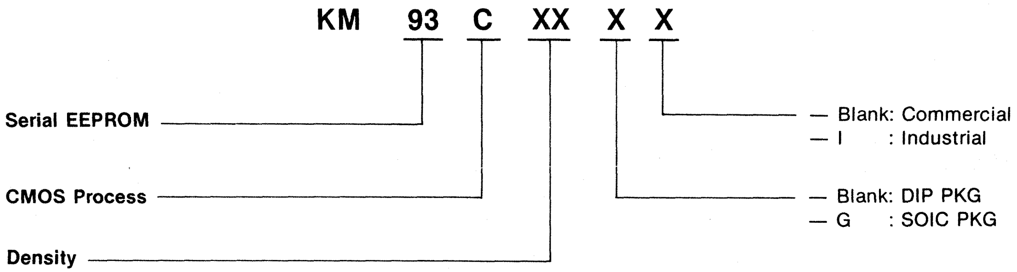
- •P: DIP
- •G: SOP
- •J : SOJ
- •T : TSOP (Standard)
- •R: TSOP (Reverse)

VERSION

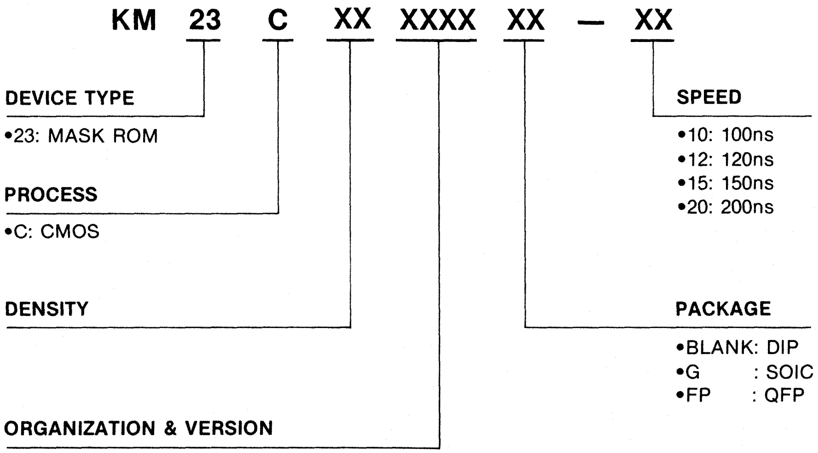
•BLANK→A→B

4.4 EEPROM





4.5 MASK ROM



4.6 FIFO

KM 75CXXA X X — XX

SAMSUNG MEMORY COMPONENT

PART NUMBER

PACKAGE

- P: Plastic DIP, 600 mil
- J : Plastic PLCC
- N: Plastic DIP, 300 mil

TEMPERATURE

- BLANK: 0~70°C
- I : −40~ +85°C

SPEED

- 12: 12ns
- 15: 15ns
- 20: 20ns
- 25: 25ns
- 35: 35ns
- 50: 50ns
- 80: 80ns

4.7 VRAM

KM 42 X X XXX X X — XX

VRAM

ORGANIZATION
- 4: X4
- 8: X8
- 16: X16

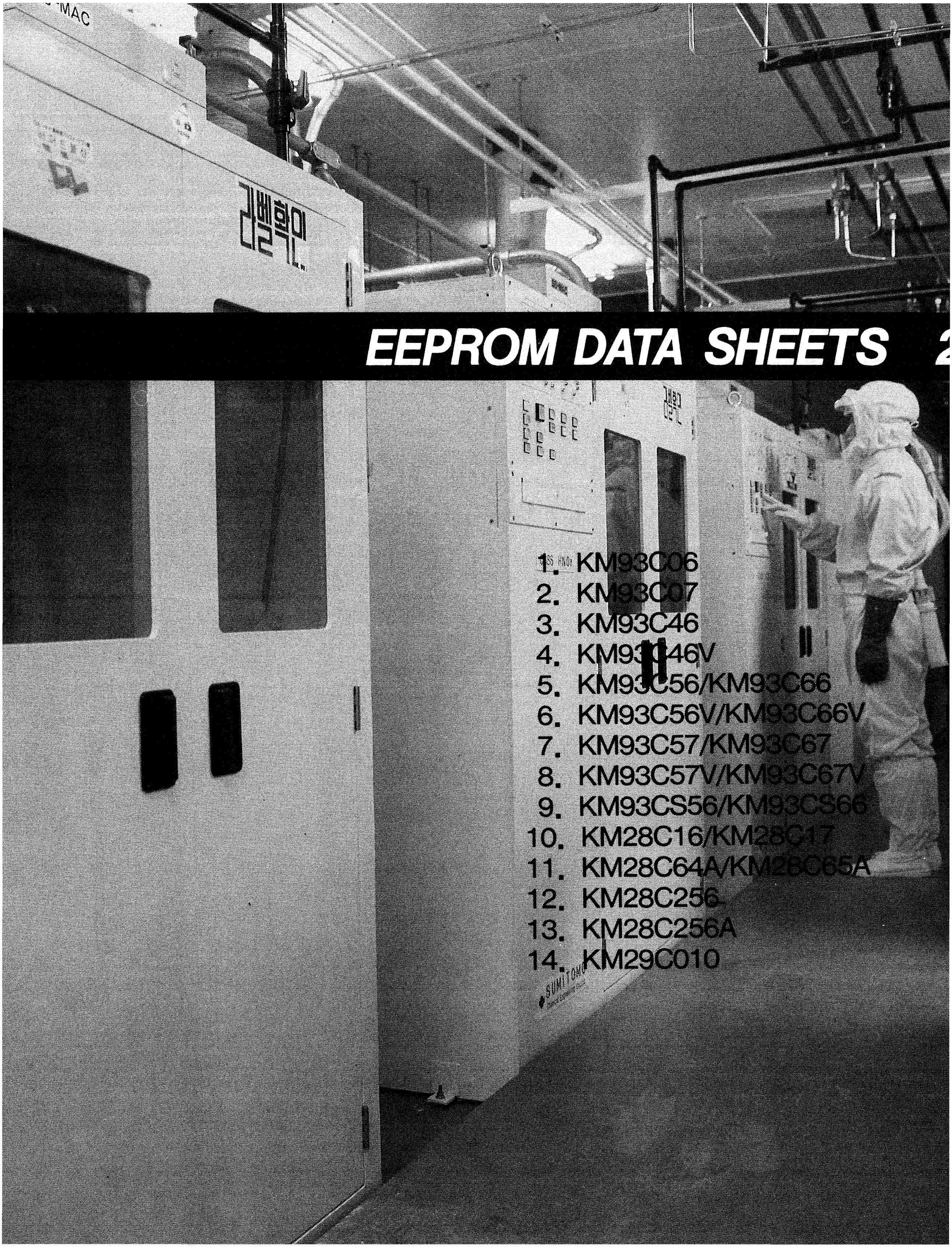
PROCESS & POWER
- C:CMOS, 5V

DENSITY
- 64K
- 128K
- 256K

DIE VERSION
- A:SECONO-UER

PACKAGE
- P: DIP
- J: SOJ
- Z: ZIP
- T: TSOP II

SPEED
- 6: 60ns
- 8: 80ns
- 10: 100ns



EEPROM DATA SHEETS 2

256-Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **KM93C06: Commercial**
  - **KM93C06I: Industrial**
- **16 × 16 serial read/write memory**
- **High performance advanced CMOS technology**
- **Reliable floating gate technology**
  - **Endurance : 100,000 cycle/byte**
  - **Data retention: 10 years**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **Standby current: 250μA (TTL)**
  - **Active current: 3 mA (TTL)**
- **TTL compatible**
- **Available in plastic DIP and SOP**

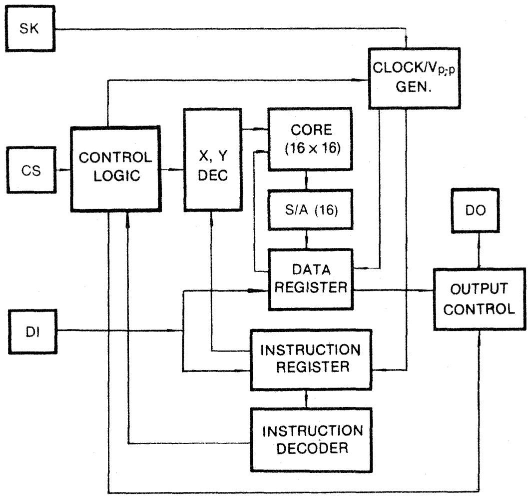
GENERAL DESCRIPTION

The KM93C06 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

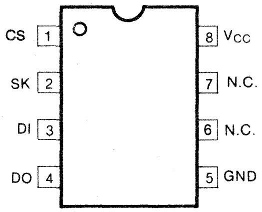
The KM93C06 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor.

The KM93C06 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

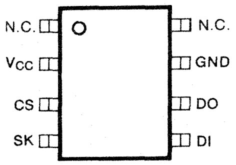
FUNCTIONAL BLOCK DIAGRAM



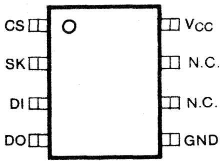
PIN CONFIGURATION



KM93C06



KM93C06G (SC06)



KM93C06GD (SC06D)

PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C06: $T_A = 0°C$ to $70°C$, Voltages referenced to V_{SS}
KM93C06I: $T_A = -40°C$ to $85°C$, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, $CS = 2.0V$, $SK = 2.0V$		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, $CS = 0.8V$		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, $CS = 0V$		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC} + 0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4 	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, $CS = 0V$		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C06 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

AC OPERATING CHARACTERISTICS

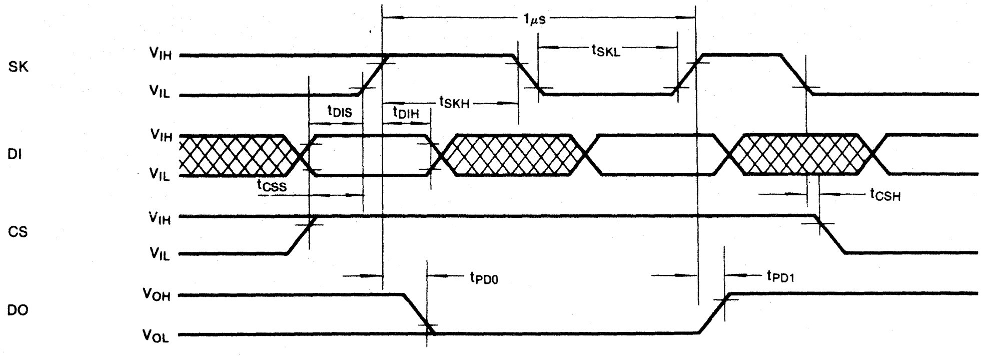
KM93C06: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM93C06I: $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$ $V_{IL} = 0.45V$, $V_{IH} = 2.4V$		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Program Cycle Time	$t_{E/W}$		10	30	ms
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of $1\mu s$, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to $1\mu s$.
e.q., if $t_{SKL} = 250ns$ then the minimum $t_{SKH} = 750ns$ in order to meet the SK frequency specification.

TIMING DIAGRAMS

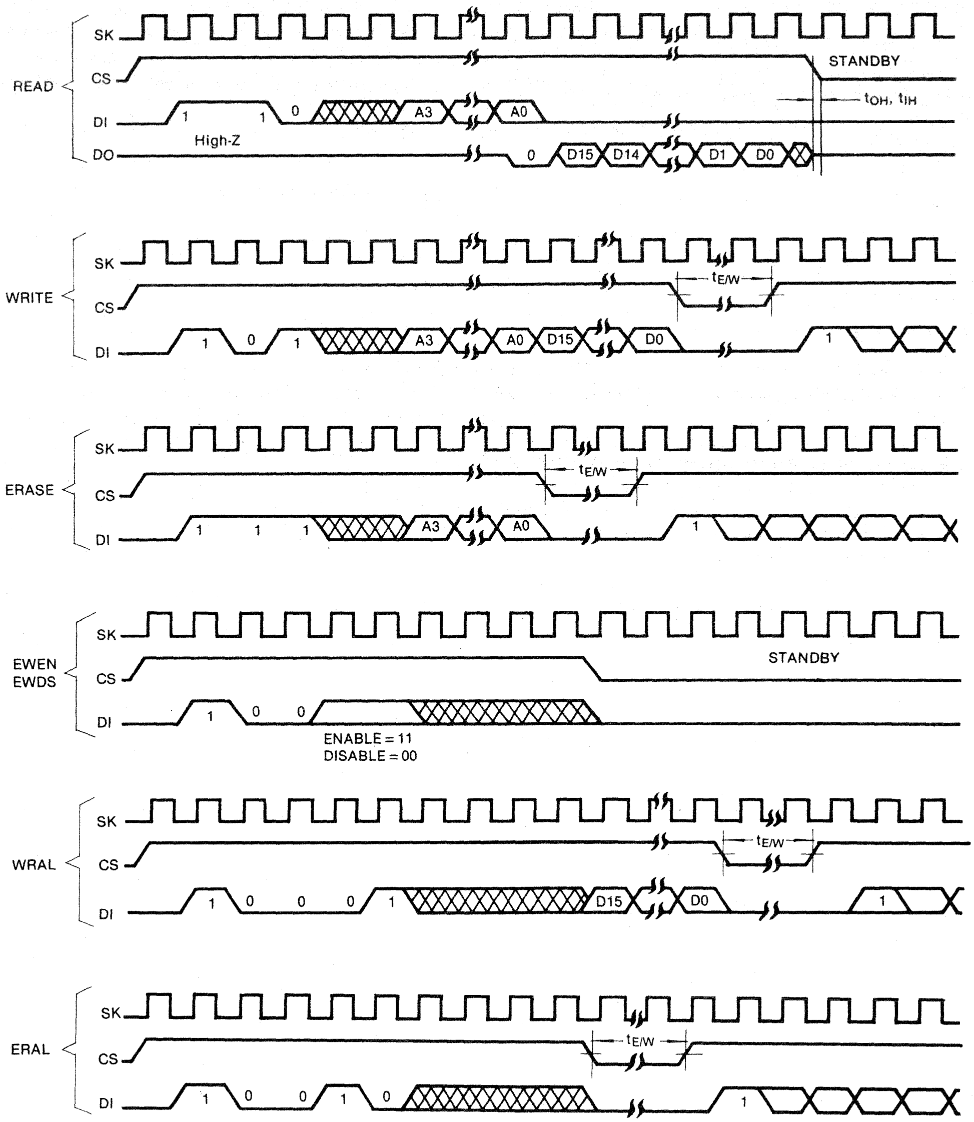
SYNCHRONOUS DATA TIMING



▨ DON'T CARE

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C06 is a 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. All the operations of the chip are preceded by an instruction set, consisting of a start bit and two OP code bits, facilitating inherent protection against false writes. The DO pin is in high-Z except for the read period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") preceds the 16 bit data output string.

EWEN / EWDS

The KM93C06 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. A chip starts an erase cycle by dropping CS low after an erase instruction and address set is input. The erase cycle is ended by raising CS input high after the program cycle time ($t_{E/W}$) is satisfied.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the write cycle. Like the erase operation, the write cycle is completed by the rising edge of the CS input.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

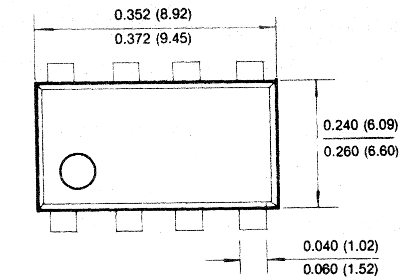
WRAL (chip write)

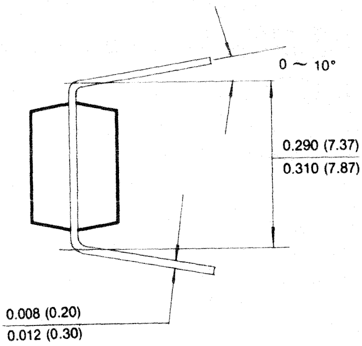
The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

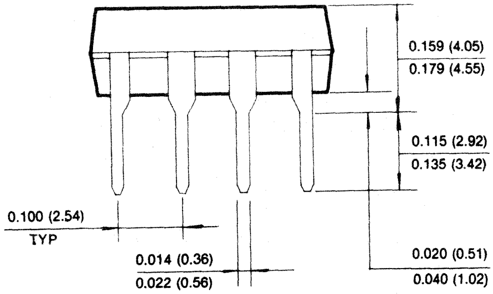
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

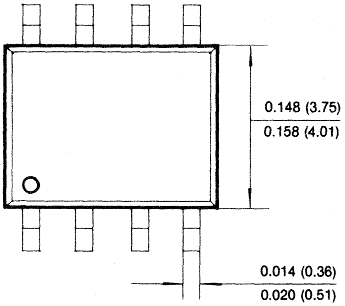
unit; inches (millimeters)

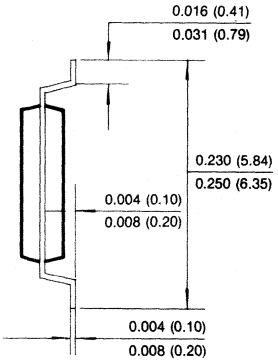


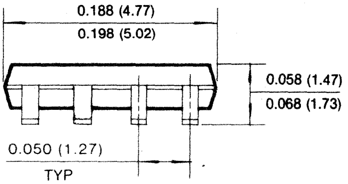




8 PIN PLASTIC SMALL OUT LINE PACKAGE







256-Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C07: Commercial**
  - **— KM93C07I: Industrial**
- **16 × 16 serial read/write memory**
- **High performance advanced CMOS technology**
- **Reliable floating gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3 mA (TTL)**
- **TTL compatible**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **Available in plastic DIP and SOP**

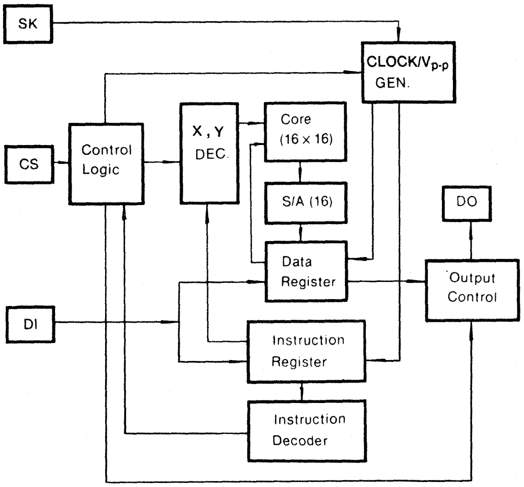
GENERAL DESCRIPTION

The KM93C07 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

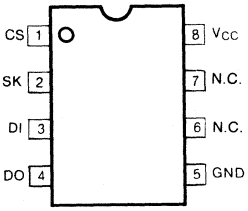
The KM93C07 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the Ready/$\overline{\text{Busy}}$ status of the device.

The KM93C07 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

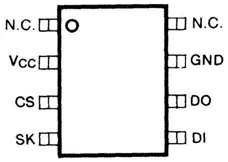
FUNCTIONAL BLOCK DIAGRAM



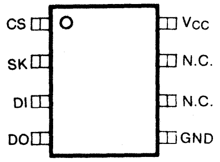
PIN CONFIGURATION



KM93C07



KM93C07G
(SC07)



KM93C07GD
(SC07D)

PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C07: $T_A = 0°C$ to $70°C$, Voltages referenced to V_{SS}
KM93C07I: $T_A = -40°C$ to $85°C$, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, $CS = 2.0V$, $SK = 2.0V$		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, $CS = 0.8V$		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, $CS = 0V$		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC} + 0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4 	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, $CS = 0V$		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C07 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

AC OPERATING CHARACTERISTICS

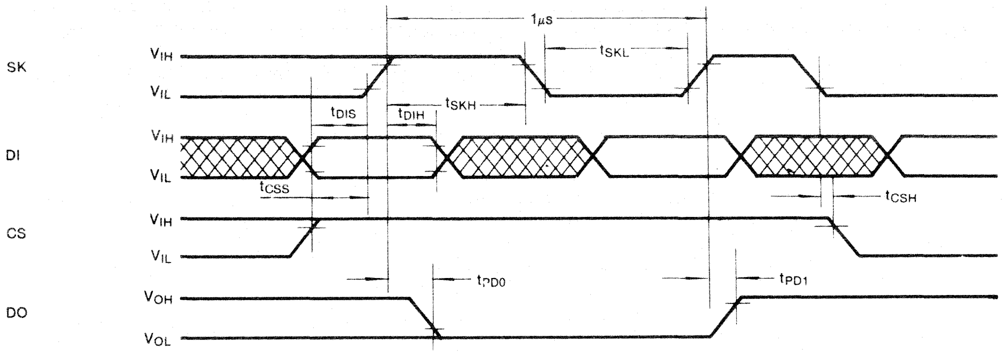
KM93C07: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM93C07I: $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$ $V_{IL} = 0.45V$, $V_{IH} = 2.4V$		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}	(Note 2)	250		ns
Rising Edge of CS to Status Valid	t_{SV}			500	ns
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1μs.
e.q., if $t_{SKL} = 250ns$ then the minimum $t_{SKH} = 750ns$ in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum 250ns(t_{CS}) between consecutive instruction cycles.

TIMING DIAGRAMS

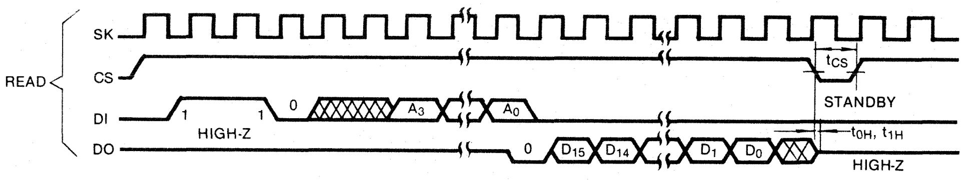
SYNCHRONOUS DATA TIMING

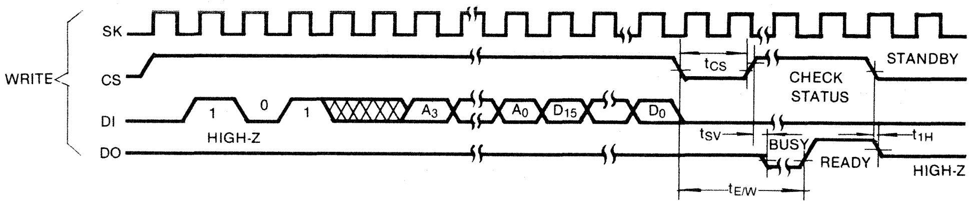


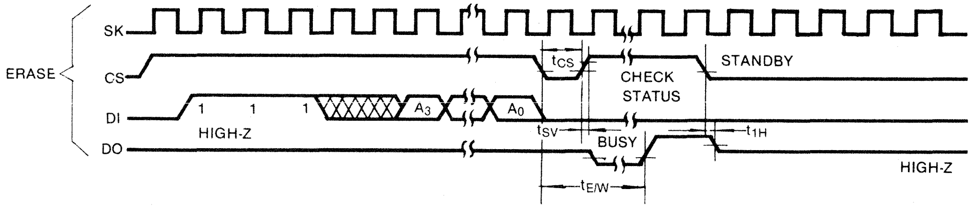
▨ DON'T CARE

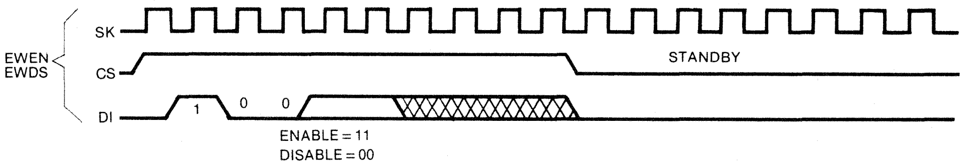
TIMING DIAGRAMS (Continued)

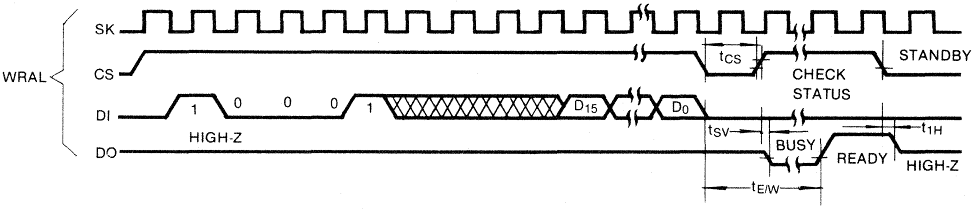
INSTRUCTION TIMING

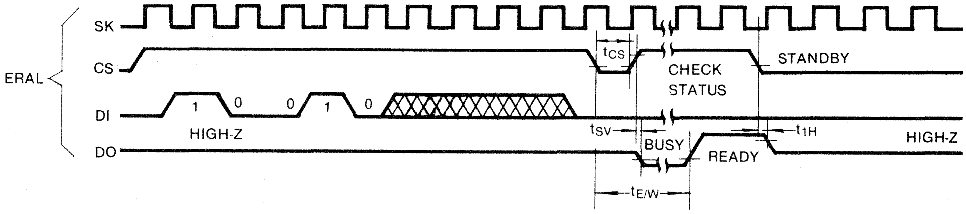












DEVICE OPERATION

The KM93C07 is a 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C07 is self-timed with the ready/$\overline{\text{busy}}$ status of the chip indicated at the DO pin. All the operations of the chip is preceded by a two OP code bits, facilitating inherent protection against false writes. The DO pin is high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C07 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts a self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{\text{busy}}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

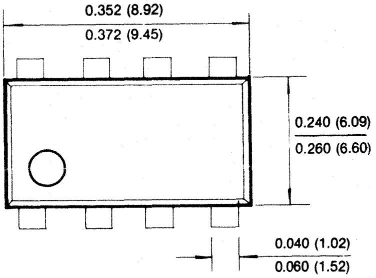
READY / $\overline{\text{BUSY}}$

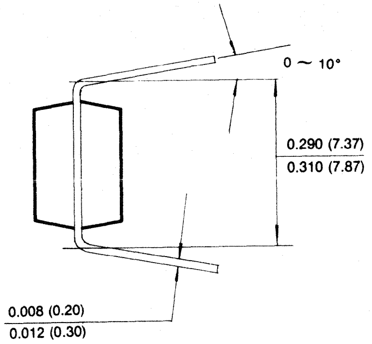
The ready/$\overline{\text{busy}}$ status of the KM93C07 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after th self-timed programming cycle has been initiated, will produces logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

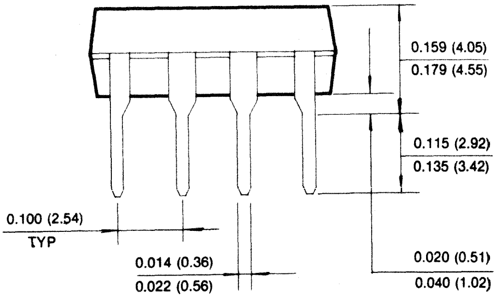
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

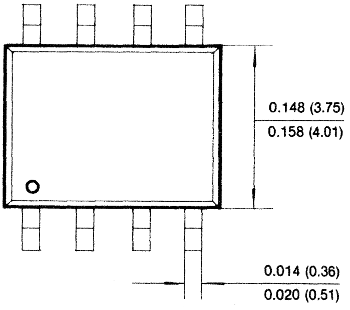
unit; inches (millimeters)

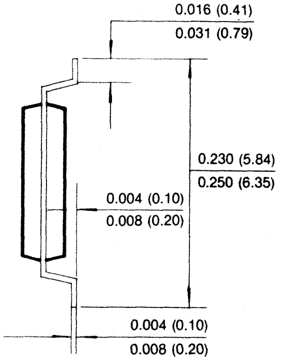


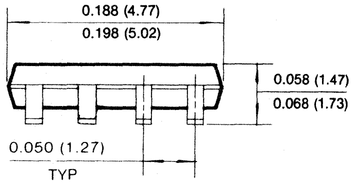




8 PIN PLASTIC SMALL OUT LINE PACKAGE







1K Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C46: Commercial**
  - **— KM93C46I: Industrial**
- **Single 5 Volt supply**
- **High performance advanced CMOS technology**
  - **— Reliable floating gate technology**
- **64 × 16 serial read/write memory**
- **TTL compatible**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3 mA (TTL)**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **100,000 Cycle Endurance**
- **Available in plastic DIP and SOP**

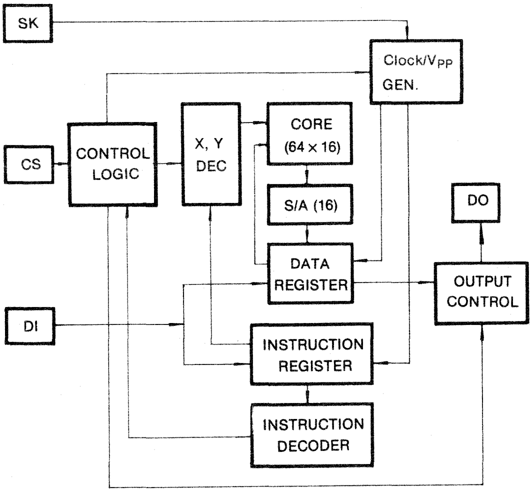
GENERAL DESCRIPTION

The KM93C46 is a CMOS 5V-Only 1,024 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

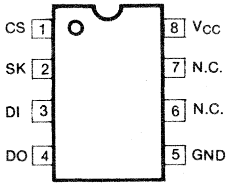
The KM93C46 is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

The KM93C46 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

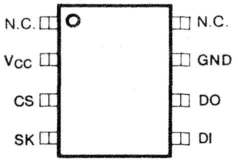
FUNCTIONAL BLOCK DIAGRAM



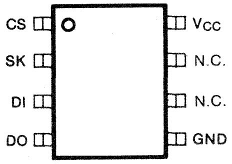
PIN CONFIGURATION



KM93C46



KM93C46G
(SC46)



KM93C46GD
(SC46D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C46 $T_A = 0$ to 70°C, Voltages referenced to V_{SS}
KM93C46I $T_A = -40$ to 85°C, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, $CS = 2.0V$, $SK = 2.0V$		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, $CS = 0.8V$		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, $CS = 0V$		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC} + 0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4 	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, $CS = 0V$		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D15-D0	Write all registers

The KM93C46 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and following 8 bits carry the OP code and the 6-bit address for 1 of 64, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

AC OPERATING CHARACTERISTICS

KM93C46 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM93C46I $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

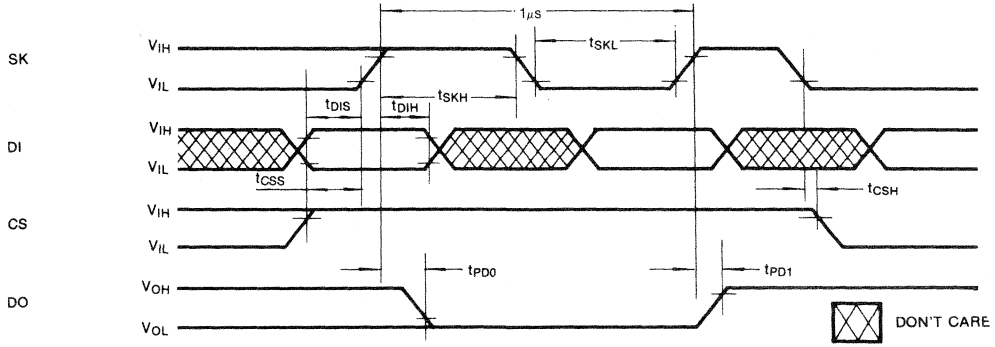
Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$ $V_{IL} = 0.45V$, $V_{IH} = 2.4V$		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Self-Timed Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}	(Note 2)	250		ns
Rising Edge of CS to Status Valid	t_{SV}			500	ns
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1μs.
e.q., if $t_{SKL} = 250ns$ then the minimum $t_{SKH} = 750ns$ in order to meet the SK frequency specification.

Note 2: CS must be brought low for a minimum 250ns(t_{CS}) between consecutive instruction cycles.

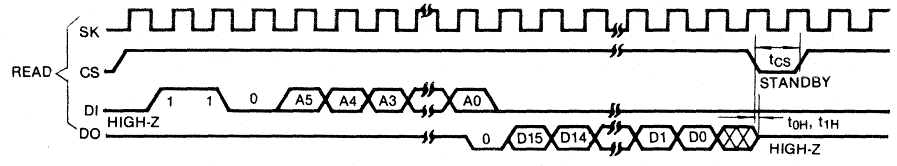
TIMING DIAGRAMS

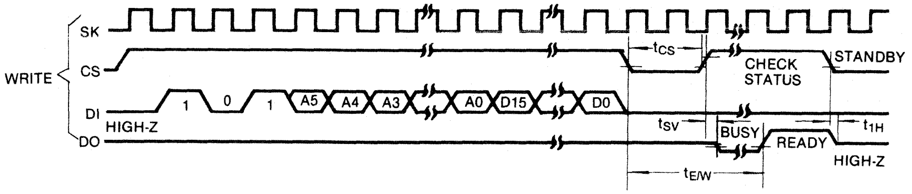
SYNCHRONOUS DATA TIMING

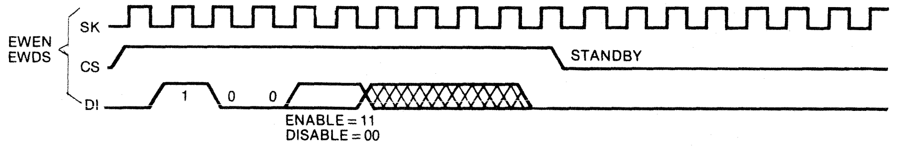


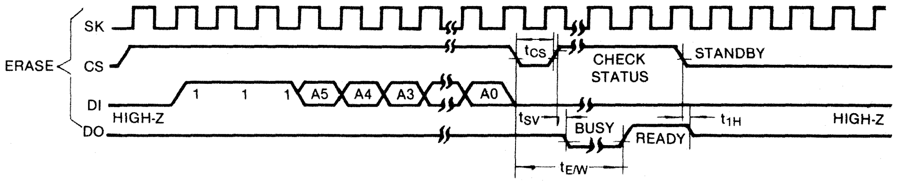
TIMING DIAGRAMS (Continued)

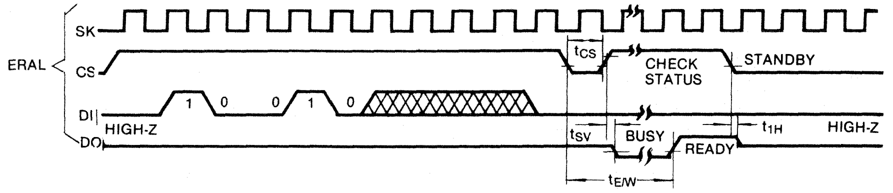
INSTRUCTION TIMING

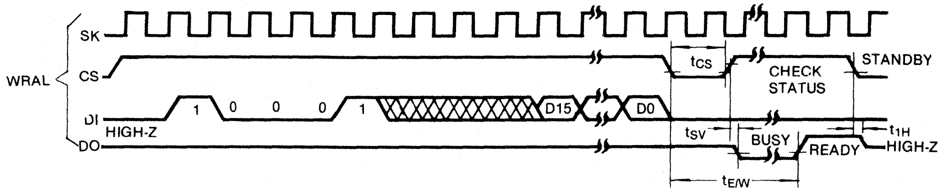












DEVICE OPERATION

The KM93C46 is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C46 is self-timed with the ready/$\overline{\text{busy}}$ status of the chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C46 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental distrubance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{\text{busy}}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array needs to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

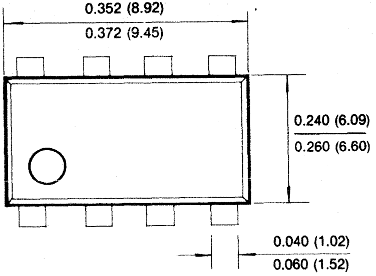
READY / $\overline{\text{BUSY}}$

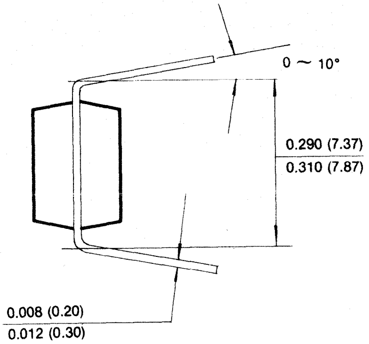
The ready/$\overline{\text{busy}}$ status of the KM93C46 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after self-timed programming cycle has been initiated, will produce logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

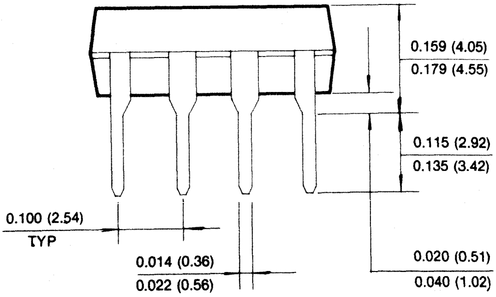
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

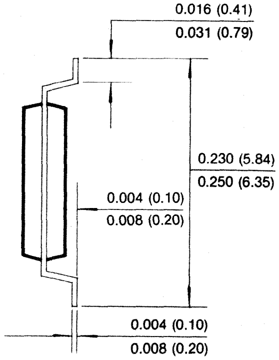
unit; inches (millimeters)

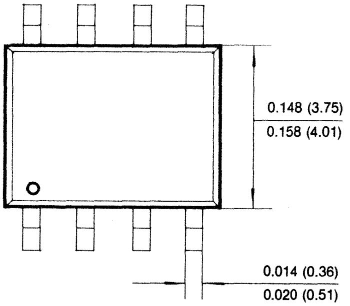


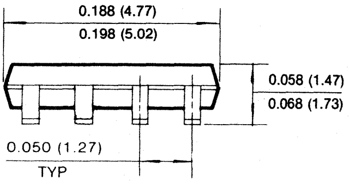




8 PIN PLASTIC SMALL OUT LINE PACKAGE







1K Bit Serial Electrically Erasable PROM

FEATURES

- Operating Temperature Range
  - — KM93C46V : Commercial
  - — KM93C46VI: Industrial
- **Enhanced extended operating voltage: 3.0V~5.5V**
- High performance Advanced CMOS Technology
  - — Reliable floating gate technology
- 64 × 16 serial read/write memory
- TTL compatible
- Low power dissipation
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3mA (TTL)**
- Self-timed programming cycle
- Device status signal during programming
- 100,000 Cycle Endurance
- Available in plastic DIP and SOP

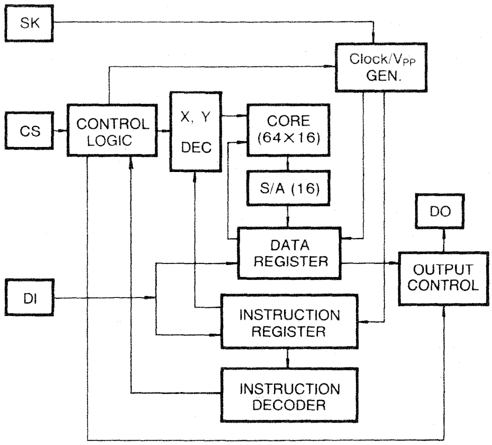
GENERAL DESCRIPTION

The KM93C46V is an extended voltage CMOS 1,024 bit nonvolatie, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

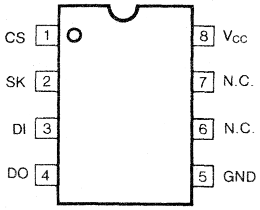
The KM93C46V is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operate in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

The KM93C46V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

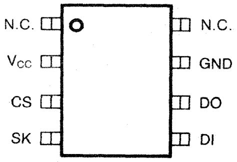
FUNCTIONAL BLOCK DIAGRAM



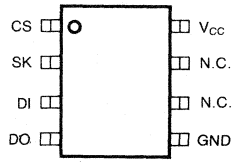
PIN CONFIGURATION



KM93C46V



KM93C46VG
(C46V)



KM93C46VGD
(C46VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C46V : Voltage reference to V_{SS}, $T_A=0°C$ to $+70°C$
KM93C46VI: Voltage reference to V_{SS}, $T_A=-40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	—	5.5	V
Ground	V_{SS}	0	0	0	V

DC CHARACTERISTICS (Recommended operating conditions otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		3.0	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC}=5.5V$, CS=2.0V, SK=2.0V	—	1	mA
Operating Current (AC)	I_{CC2}	$V_{CC}=5.5V$, fsk=250KHz	—	3	mA
Standby Current (TTL)	I_{SB1}	$4.5 \leqslant V_{CC} \leqslant 5.5$, CS=0.8V	—	250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC}=5.5V$, CS=0V	—	100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels ($4.5 \leqslant V_{CC} \leqslant 5.5$)	V_{OL1} V_{OH1}	$I_{OL}=2.1mA$ $I_{OH}=-400\mu A$	— 2.4	0.4 —	V V
Output Voltage Levels ($3.0V \leqslant V_{CC} \leqslant 4.5$)	V_{OL2} V_{OH2}	$I_{OL}=10\mu A$ $I_{OH}=-10\mu A$	— 1.5	0.2 —	V V
Input Leakage Current	I_{LI}	$V_{IN}=5.5V$	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=5.5$, CS=0V	—	10	μA

INDTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D_{15}-D_0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D_{15}-D_0	Write all registers

The KM93C46V provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and following 8 bits carry the OP code and the 6-bit address for 1 of 64, 16-bit registers.

AC TEST CONDITIONS

Parameter		Value
Input Pulse Levels		0.2V to 2.6V
Input Rise and Fall Times		20ns
Timing Measurement Reference Level	Input	0.8V and 2.0V
	Output	0.8V and 1.5V
Output Load		1 TTL GATE and CL=100 pF

AC OPERATING CHARACTERISTICS

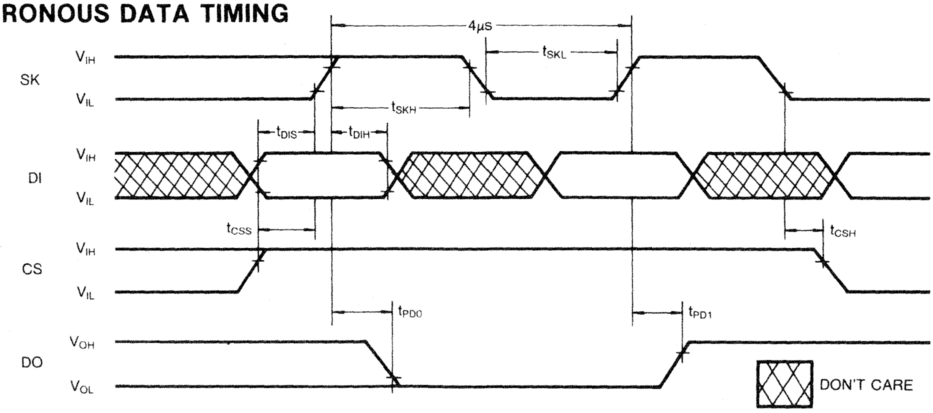
KM93C46V : $T_A=0°C$ to $+70°C$
KM93C46VI: $T_A=-40°C$ to $+85°C$

Parameter	Symbol	Conditions	Min	Max	Unit
SK Frequency		—	0	250	KHz
SK High Time	t_{SKH}	—	1	—	μs
SK Low Time	t_{SKL}	—	1	—	μs
Chip Select Setup Time	t_{CSS}	—	0.2	—	μs
Chip Select Hold Time	t_{CSH}	—	0	—	μs
Data Setup Time	t_{DIS}	—	0.4	—	μs
Data Hold Time	t_{DIH}	—	0.4	—	μs
Output High Delay Time	t_{PD1}	$V_{OL}=0.8V$, $V_{OH}=1.5V$ $V_{IL}=0.2V$, $V_{IH}=2.6V$	—	2	μs
Output Low Delay Time	t_{PD0}		—	2	μs
Self-Timed Program Cycle Time	$t_{E/W1}$ $t_{E/W2}$	$4.5 \leqslant V_{CC} \leqslant 5.5V$ $3.0 \leqslant V_{CC} \leqslant 4.5$	— —	10 15	ms ms
Min CS Low Time	t_{CS}	—	1	—	μs
Rising Edge of CS to Status Valid	t_{SV}	—	—	1	μs
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{1H}	—	—	0.4	μs

Notes: 1 The SK frequency spec. specifies a minimum SK clock period of 4μs, therefore in a SK clock $t_{SKH}+t_{SKL}$ must be greater than or equal to 4μs.
2. CS must be brought low for a minimum 1μs (t_{CS}) between consecutive instruction cycles.

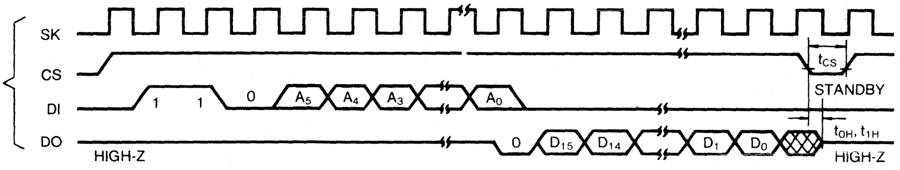
TIMING DIAGRAMS

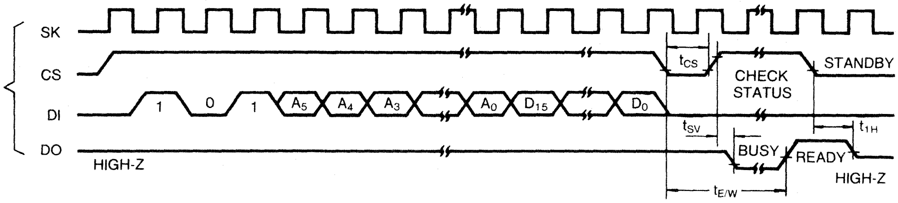
SYNCHRONOUS DATA TIMING

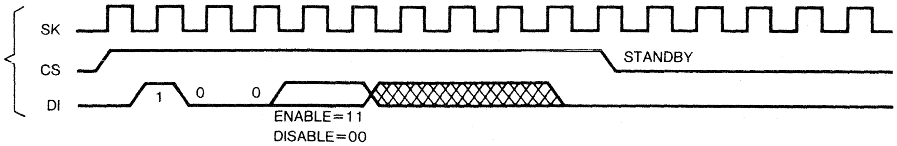


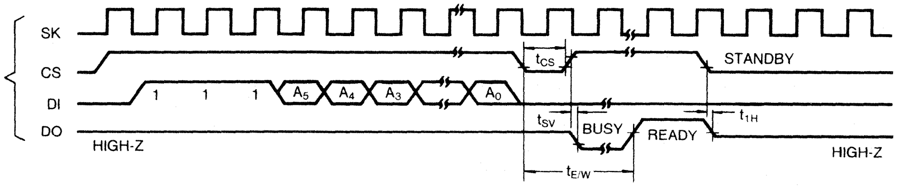
TIMING DIGRAMS (Continued)

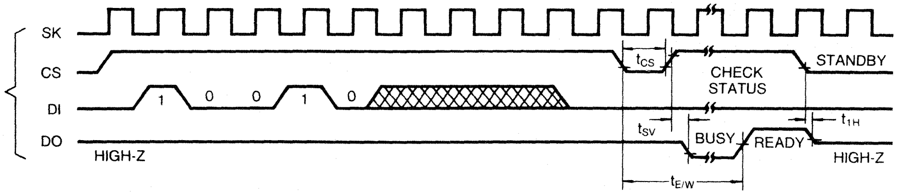
INSTRUCTION TIMING

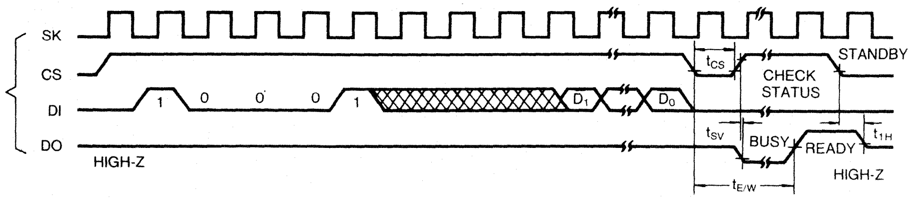

READ


WRITE


EWEN
EWDS


ERASE


ERAL


WRAL

DEVICE OPERATION

The KM93C46V is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a 3.0V to 5.5V single power supply. The erase and write cycle of the KM93C46V is self-timed with the read/$\overline{\text{busy}}$ status of the chip indicated at the D0 pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The D0 pin is high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C46V is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until a erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low befor the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{\text{busy}}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e, logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is indentical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array needs to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

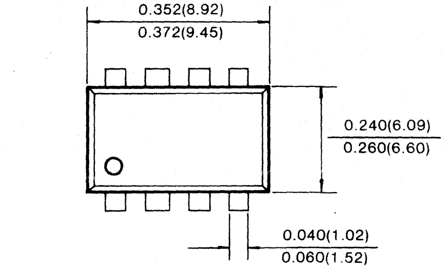
READY/$\overline{\text{BUSY}}$

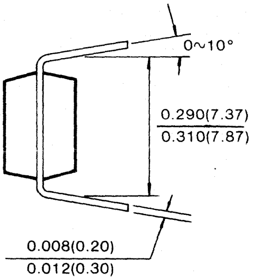
The ready/$\overline{\text{busy}}$ state of the KM93C46V during all the selftimed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after self-timed programming cycle has been initiated, will produce logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

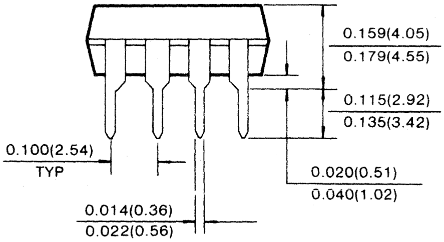
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

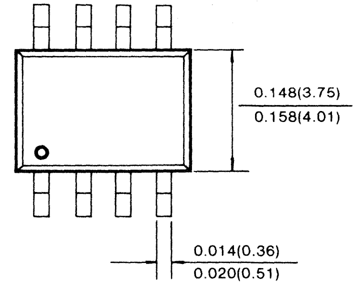
unit; inches (millimeters)

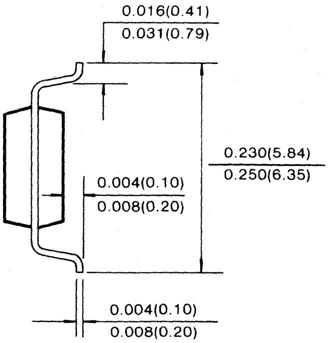


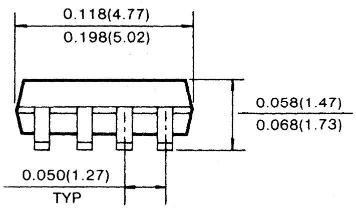




8 PIN PLASTIC SMALL OUT LINE PACKAGE







KM93C56/KM93C66

PRELIMINARY
CMOS EEPROM

2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 100 μA (TTL)**
- **Memory organization:**
  - **— 128 × 16 bits for KM93C56**
  - **— 256 × 16 bits for KM93C66**
- **System Clock Frequency: 1 MHz (max.)**
- **Self timed write cycle**
  - **— Automatic erase before write**
  - **— R/B status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**

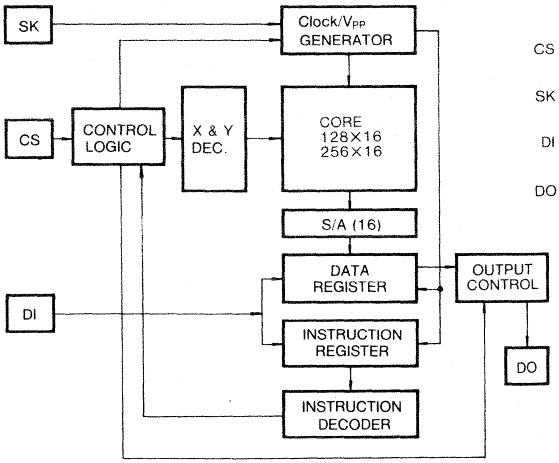
GENERAL DESCRIPTION

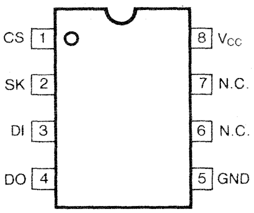
The KM93C56/66 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

The KM93C56/66 can be organized as 128/256 registers of 16 bits each, which can be read/written serially by a microprocessor.

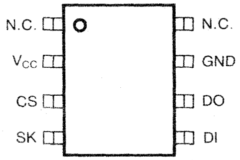
The KM93C56/66 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

FUNCTIONAL BLOCK DIAGRAM

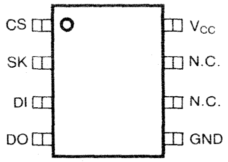




KM93C56/66



KM93C56G/66G
(SC56/66)



KM93C56GD/66GD
(SC56D/66D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
V$_{CC}$	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	100	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	50	μA
Input Low Voltage Levels		V_{IL}		—	0.8	V
Input High Voltage Levels		V_{IH}		2.0	—	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	—	10	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	—	10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A7A6A5A4A3A2A1A0	D_{OUT}	Read register at specified address
WRITE	1	01	A7A6A5A4A3A2A1A0	D_{15}-D_0	Write the data at specified address
ERASE	1	11	A7A6A5A4A3A2A1A0	—	Erase the data at specified address
EWEN	1	00	11XXXXXX	—	Erase/Write enable
EWDS	1	00	00XXXXXX	—	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	Write all registers
ERAL	1	00	10XXXXXX	—	Erase all registers

Note: 1. A7 is a "don't care" address for KM93C56.

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

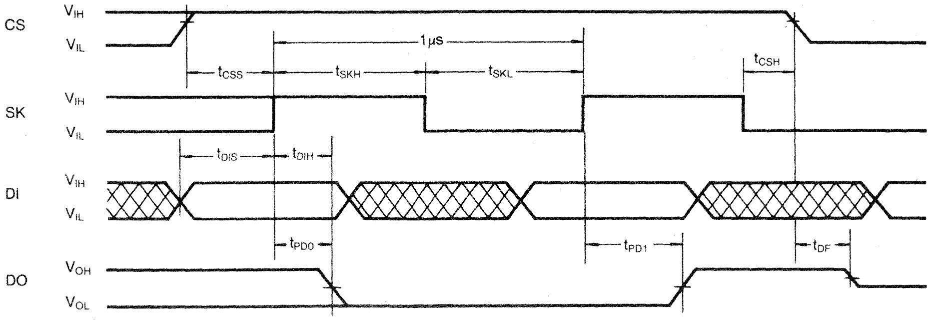
AC OPERATING CHARACTERISTICS (V_{CC}= 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output delay to data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

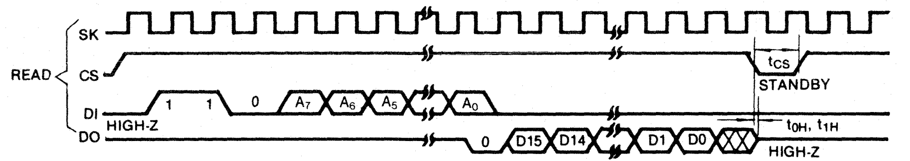
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

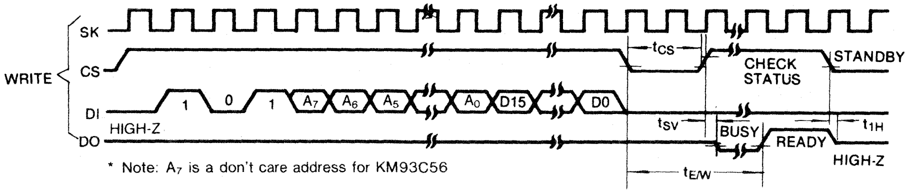


TIMING DIAGRAMS (Continued)

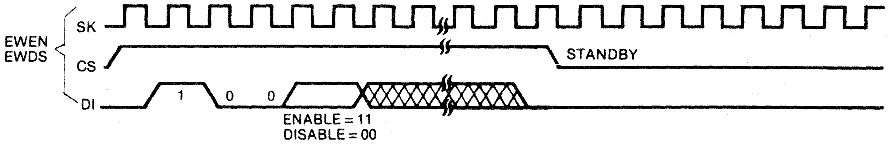
INSTRUCTION TIMING

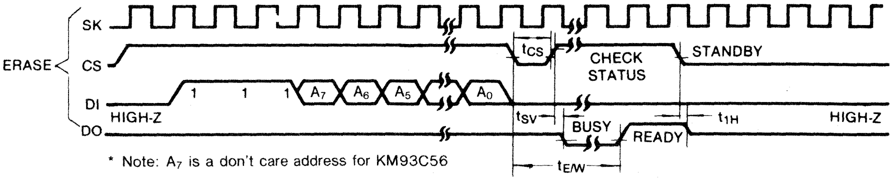


* Note: A_7 is a don't care address for KM93C56

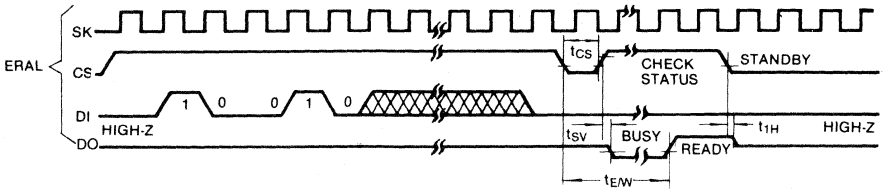


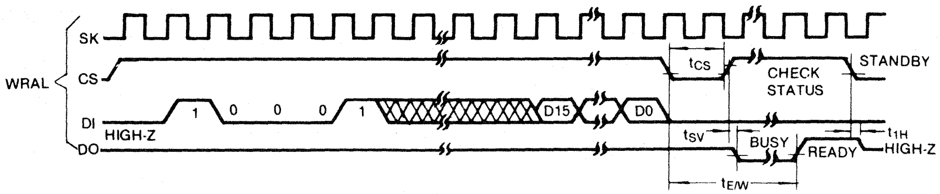
* Note: A_7 is a don't care address for KM93C56





* Note: A_7 is a don't care address for KM93C56





INTRODUCTION

The KM93C56/66 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93C56/66 is self timed with the ready/$\overline{\text{busy}}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C66/56 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are written simultaneously with given data.

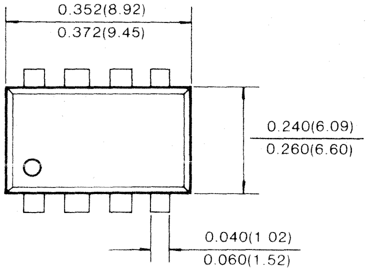
ERAL

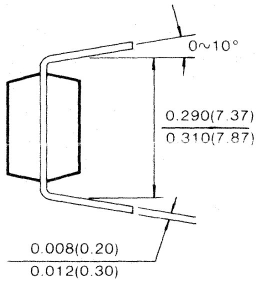
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

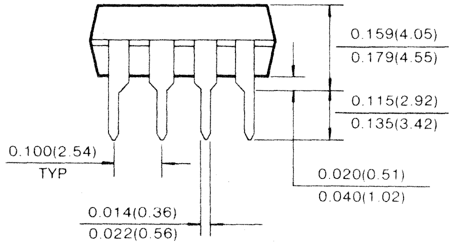
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

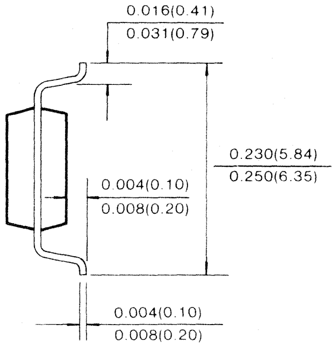
unit; inches (millimeters)

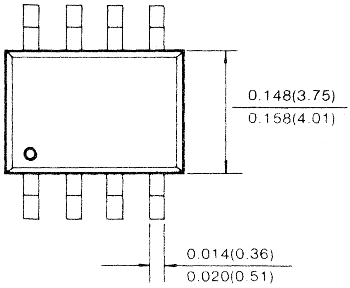


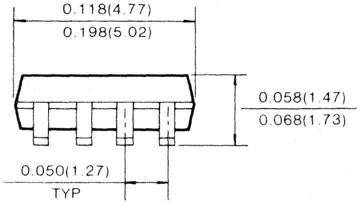




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Enhanced extended operating voltage: 2.0V ~ 4.5V**
- **Low power consumption**
  - **Active: 2 mA (TTL)**
  - **Standby: 100 μA (TTL)**
- Memory organization:
  - 128 × 16 bits for KM93C56V
  - 256 × 16 bits for KM93C66 V
- System Clock Frequency: 1 MHz (max.)
- Self timed write cycle
  - Automatic erase before write
  - R/B status signal during programming
- Reliable CMOS floating-gate technology
  - Endurance : 100,000 cycle/byte
  - Data retention: 10 years

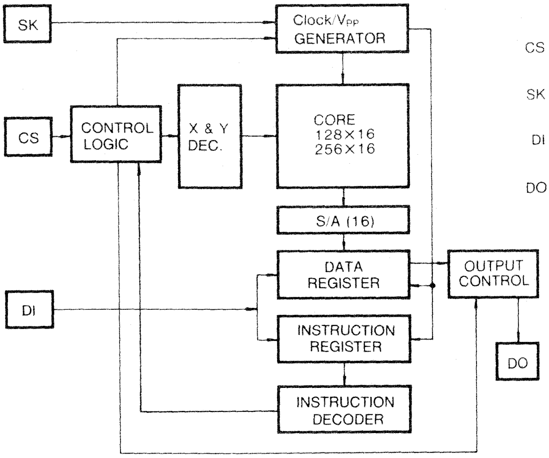
GENERAL DESCRIPTION

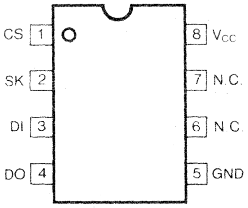
The KM93C56V/66V is a extended voltage 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

The KM93C56V/66V can be organized as 128/256 registers of 16 bits each, which can be read/written serially by a microprocessor.

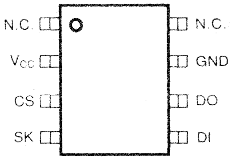
The KM93C56V/66V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

FUNCTIONAL BLOCK DIAGRAM

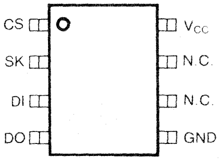




KM93C56V/66V



KM93C56VG/66VG
(C56V/66V)



KM93C56VGD/66VGD
(C56VD/66VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	3.0	4.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC}=2.0V to 4.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		2.0	4.5	V
Operating Current	DC	I_{CC1}	$CS=V_{IH}$, $SK=V_{IH}$	—	1	mA
	AC	I_{CC2}	$CS=V_{IH}$, SK=1.0MHz	—	2	mA
Standby Current	TTL	I_{SB1}	V_{CC}=4.5V, $CS=V_{IL}$	—	100	μA
	CMOS	I_{SB2}	V_{CC}=4.5V, $CS=V_{SS}$	—	50	μA
Input Low Voltage Levels		V_{IL}		—	0.3	V
Input High Voltage Levels		V_{IH}		V_{CC}-0.3	—	V
Output Voltage Levels		V_{OL}	$I_{OL}=10\mu A$	—	0.2	V
		V_{OH}	$I_{OH}=-10\mu A$	V_{CC}-0.2	—	V
Input Leakage Current		I_{IL}	V_{IN}=4.5V	—	10	μA
Output Leakage Current		I_{OL}	V_{OUT}=4.5V, CS=0V	—	10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A7A6A5A4A3A2A1A0	D_{OUT}	Read register at specified address
WRITE	1	01	A7A6A5A4A3A2A1A0	D_{15}-D_0	Write the data at specified address
ERASE	1	11	A7A6A5A4A3A2A1A0	—	Erase the data at specified address
EWEN	1	00	11XXXXXX	—	Erase/Write enable
EWDS	1	00	00XXXXXX	—	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	Write all registers
ERAL	1	00	10XXXXXX	—	Erase all registers

Note: 1. A7 is a "don't care" address for KM93C56V.

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.3V to $V_{CC}-0.3V$
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

AC OPERATING CHARACTERISTICS (V_{CC}=2.0V to 4.5V unless otherwise specified)

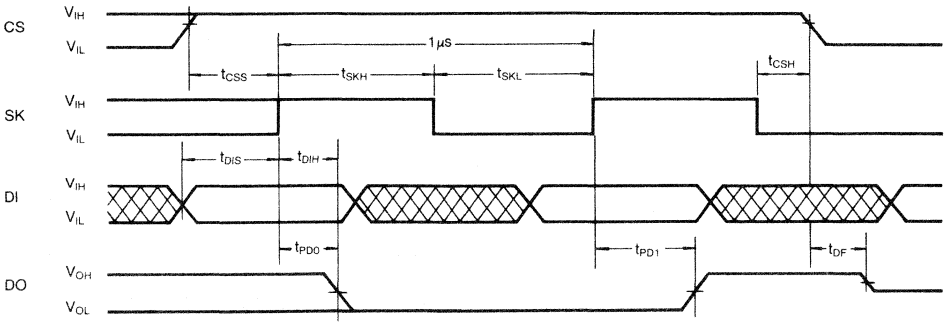
Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output delay to data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

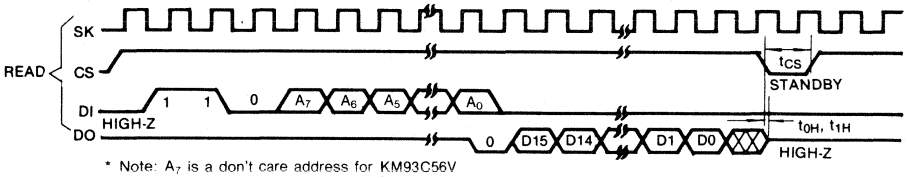
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

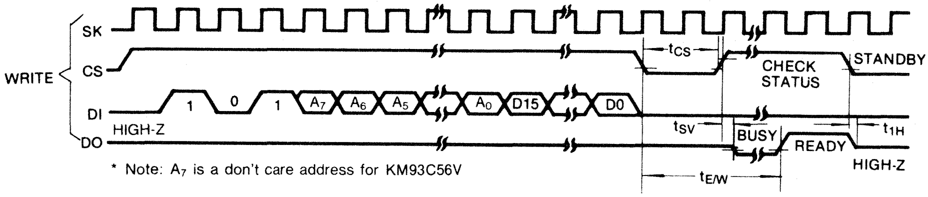


TIMING DIAGRAMS (Continued)

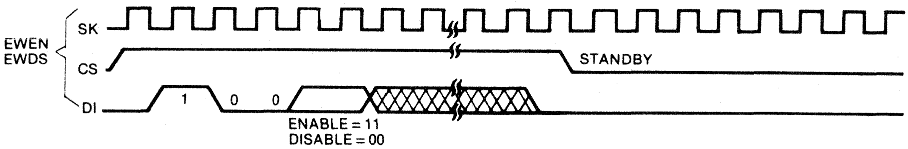
INSTRUCTION TIMING

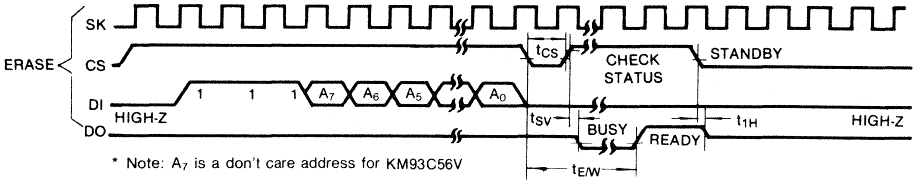


* Note: A_7 is a don't care address for KM93C56V

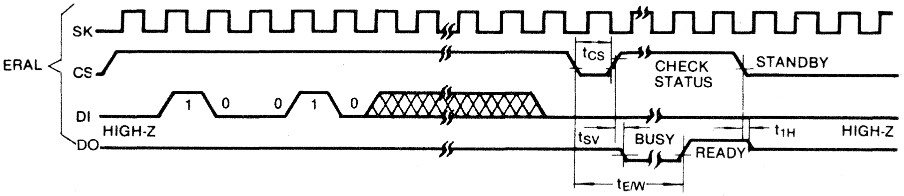


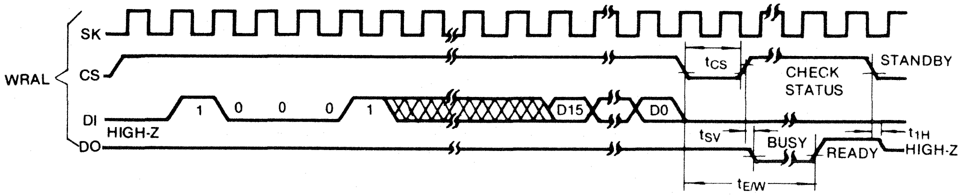
* Note: A_7 is a don't care address for KM93C56V





* Note: A_7 is a don't care address for KM93C56V





INTRODUCTION

The KM93C56V/66V is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a 2.0V to 4.5V single power supply. The write cycle of the KM93C56V/66V is self timed with the ready/$\overline{\text{busy}}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C66/56 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are written simultaneously with given data.

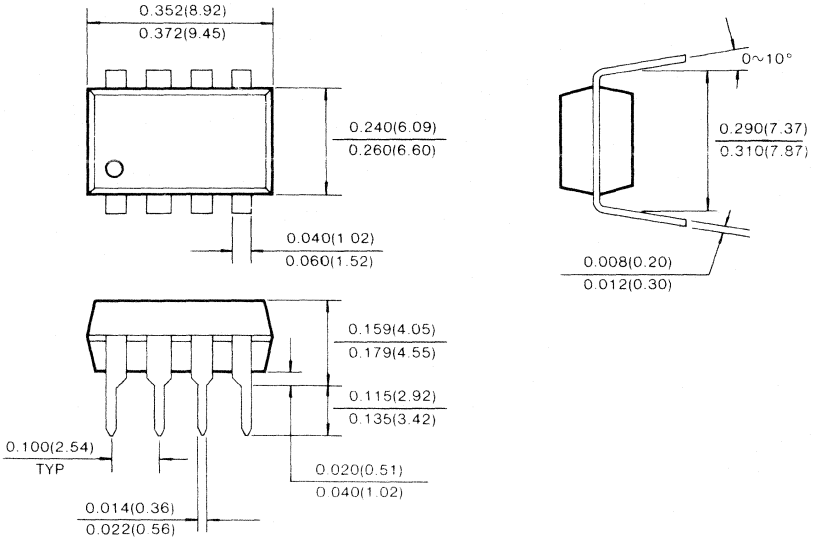
ERAL

The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

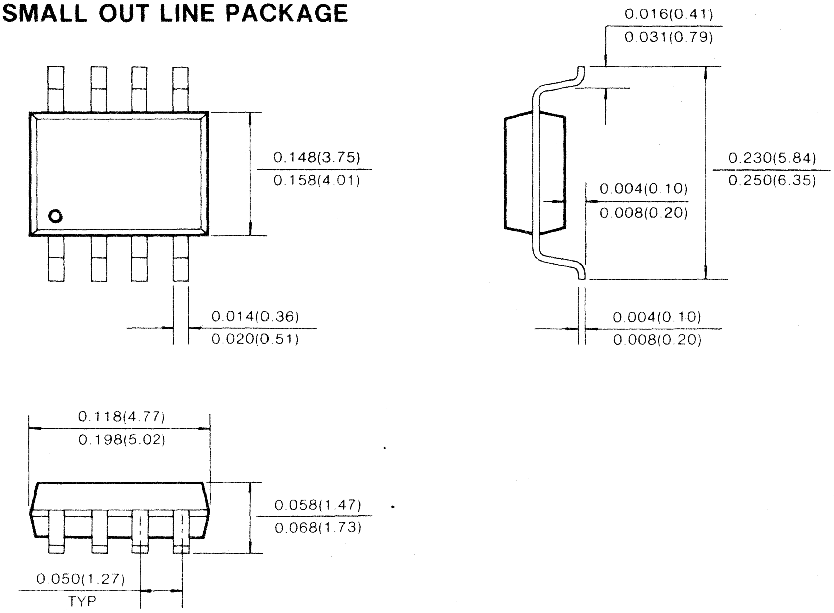
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



KM93C57/KM93C67

PRELIMINARY
CMOS EEPROM

2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 100 μA (TTL)**
- **User selectable memory organization**
  - **— 256 × 16 or 512 × 8 for KM93C67**
  - **— 128 × 16 or 256 × 8 for KM93C57**
- **System Clock Frequency: 1 MHz (max.)**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**

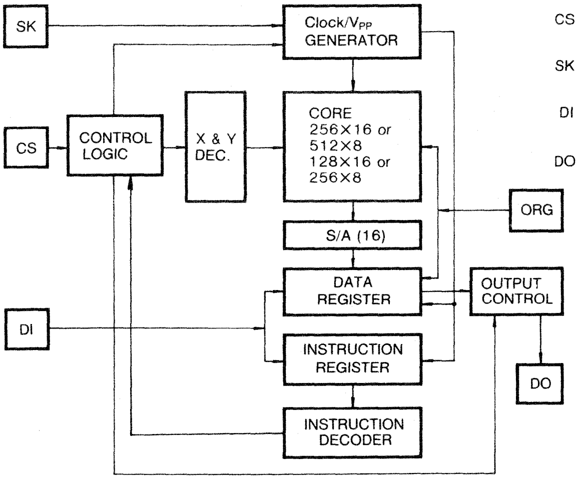
GENERAL DESCRIPTION

The KM93C57/67 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

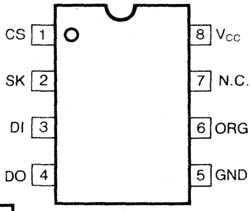
The KM93C57/67 can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

The KM93C57/67 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

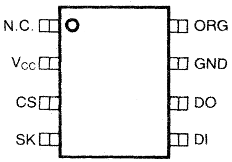
FUNCTIONAL BLOCK DIAGRAM



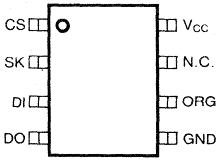
PIN CONFIGURATION



KM93C57/67



KM93C57G/67G
(SC57/67)



KM93C57GD/67GD
(SC57D/67D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	100	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	50	μA
Input Low Voltage Levels		V_{IL}		—	0.8	V
Input High Voltage Levels		V_{IH}		2.0	—	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	—	10	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	—	10	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and $C_L=100pF$

AC OPERATING CHARACTERISTICS

($V_{CC}=4.5V$ to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if $t_{SKL}=250$ ns then the minimum $t_{SKH}=750$ ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

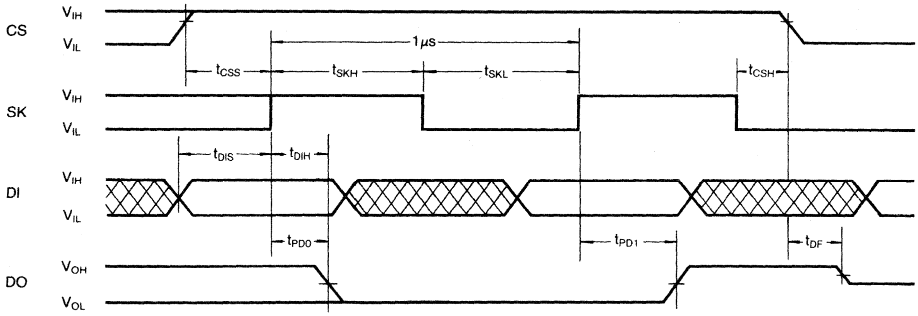
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 × 16 *(128 × 16)	512 × 8 (256 × 8)	256 × 16	512 × 8	
READ	1	10	A7~A0 (A6~A0)	A8~A0 (A7~A0)	DOUT (16 bit)	DOUT (8 bit)	Read register at specified address
WRITE	1	01	A7~A0 (A6~A0)	A8~A0 (A7~A0)	$D_{15} \sim D_0$	$D_8 \sim D_0$	Write the data at specified address
ERASE	1	11	A7~A0 (A6~A0)	A8~A0 (A7~A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	$D_8 \sim D_0$	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '(   )' is appliable to KM93C57

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

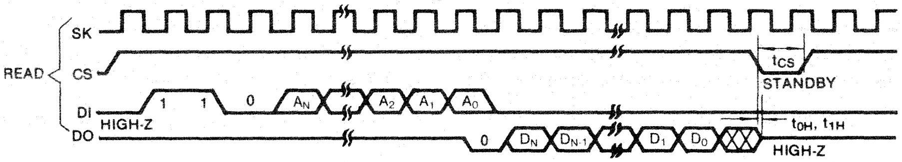


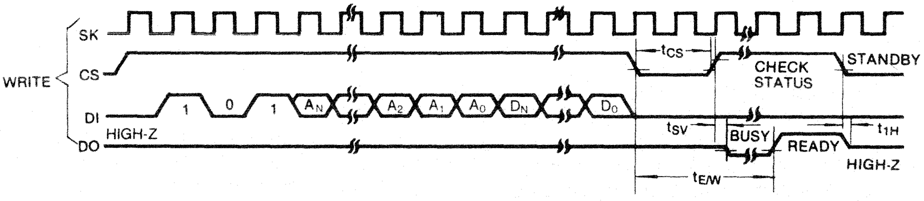
ORGANIZATION

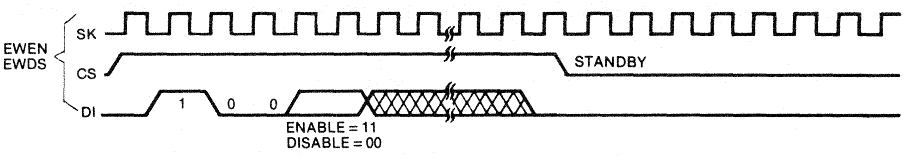
P/N	Organization	AN	DN
KM93C67	512× 8	A_8	D_7
	256×16	A_7	D_{15}
KM93C57	256× 8	A_7	D_7
	128×16	A_6	D_{15}

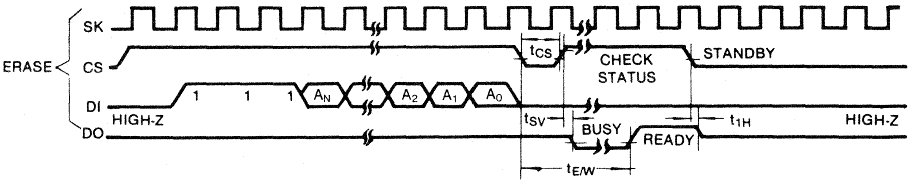
TIMING DIAGRAMS (Continued)

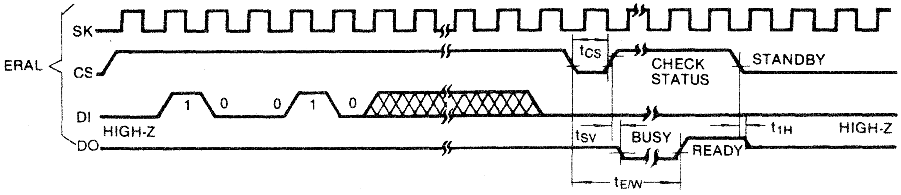
INSTRUCTION TIMING

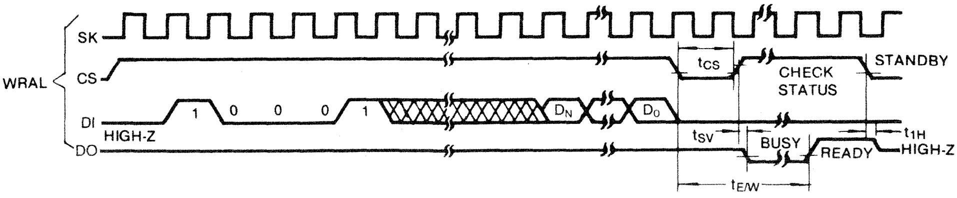












INTRODUCTION

The KM93C57/67 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93C57/67 is self timed with the ready/$\overline{\text{busy}}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

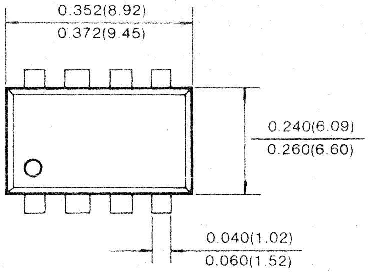
ERAL

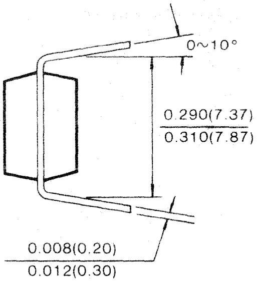
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

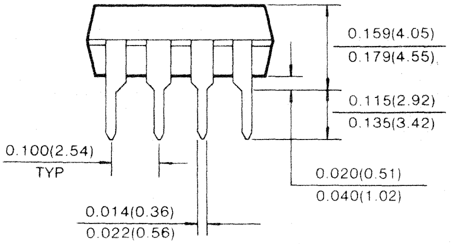
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

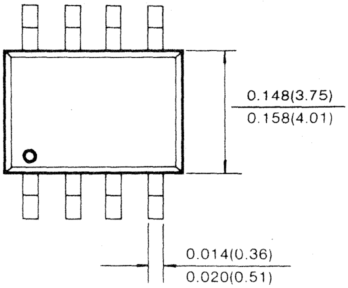
unit; inches (millimeters)

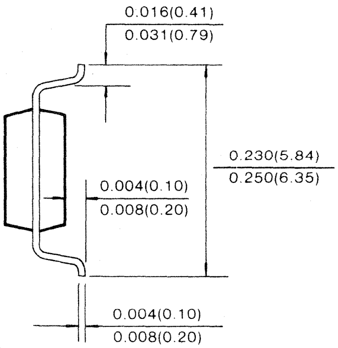


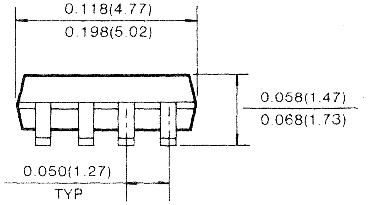




8 PIN PLASTIC SMALL OUT LINE PACKAGE







KM93C57V/KM93C67V

PRELIMINARY CMOS EEPROM

2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Enhanced extended operating voltage: 2.0V ~ 4.5V**
- **Low power consumption**
  - **Active: 2 mA (TTL)**
  - **Standby: 100 μA (TTL)**
- User selectable memory organization
  - 256 × 16 or 512 × 8 for KM93C67V
  - 128 × 16 or 256 × 8 for KM93C57V
- System Clock Frequency: 1 MHz (max.)
  - Automatic erase before write
  - R/$\overline{B}$ status signal during programming
- Reliable CMOS floating-gate technology
  - Endurance : 100,000 cycle/byte
  - Data retention: 10 years

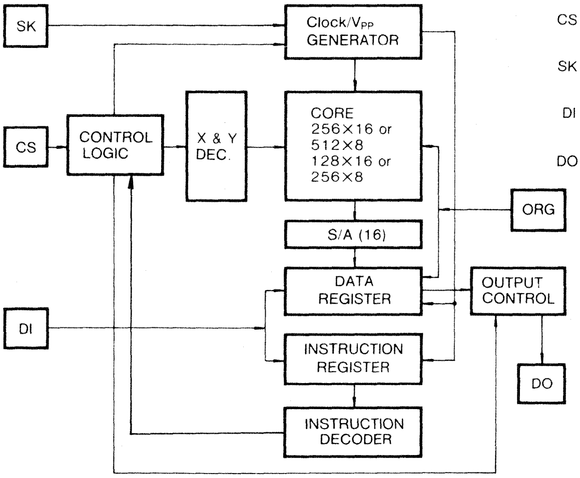
GENERAL DESCRIPTION

The KM93C57V/67V is a extended voltage 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

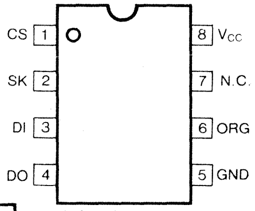
The KM93C57V/67V can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

The KM93C57V/67V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

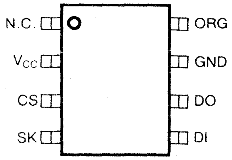
FUNCTIONAL BLOCK DIAGRAM



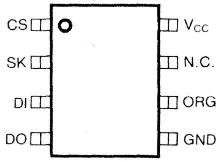
PIN CONFIGURATION



KM93C57V/67V



KM93C57VG/67VG (C57V/67V)



KM93C57VGD/67VGD (C57VD/67VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	3.0	4.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 2.0V to 4.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		2.0	4.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	2	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 4.5V, CS = V_{IL}	—	100	μA
	CMOS	I_{SB2}	V_{CC} = 4.5V, CS = V_{SS}	—	50	μA
Input Low Voltage Levels		V_{IL}		—	0.3	V
Input High Voltage Levels		V_{IH}		V_{CC}-0.3	—	V
Output Voltage Levels		V_{OL}	I_{OL} = 10μA	—	0.2	V
		V_{OH}	I_{OH} = −10μA	V_{CC}-0.2	—	V
Input Leakage Current		I_{IL}	V_{IN} = 4.5V	—	10	μA
Output Leakage Current		I_{OL}	V_{OUT} = 4.5V, CS = 0V	—	10	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.3V to $V_{CC} - 0.3V$
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and $C_L = 100pF$

AC OPERATING CHARACTERISTICS

($V_{CC} = 2.0V$ to 4.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if $t_{SKL}=250$ ns then the minimum $t_{SKH}=750$ ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

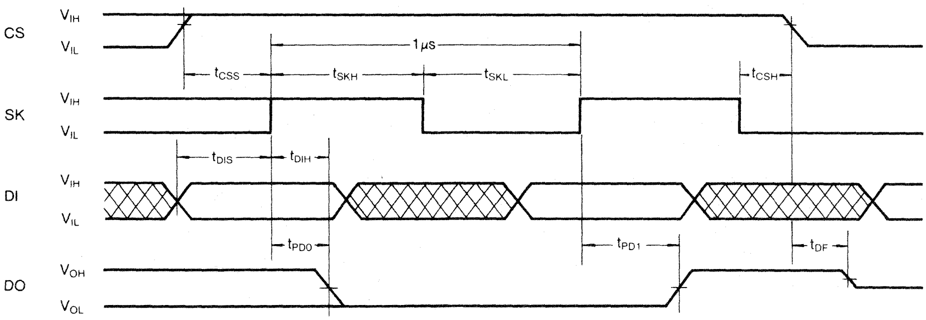
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 × 16 *(128 × 16)	512 × 8 (256 × 8)	256 × 16	512 × 8	
READ	1	10	A7∼A0 (A6∼A0)	A8∼A0 (A7∼A0)	D_{OUT} (16 bit)	D_{OUT} (8 bit)	Read register at specified address
WRITE	1	01	A7∼A0 (A6∼A0)	A8∼A0 (A7∼A0)	D_{15}∼D_0	D_8∼D_0	Write the data at specified address
ERASE	1	11	A7∼A0 (A6∼A0)	A8∼A0 (A7∼A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	D_8∼D_0	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '(   )' is appliable to KM93C57V

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

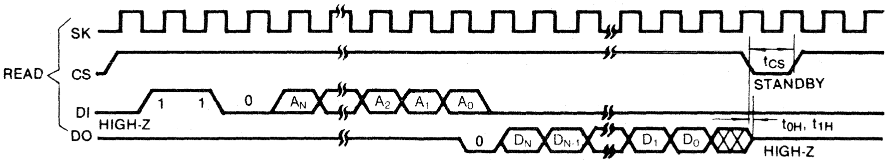


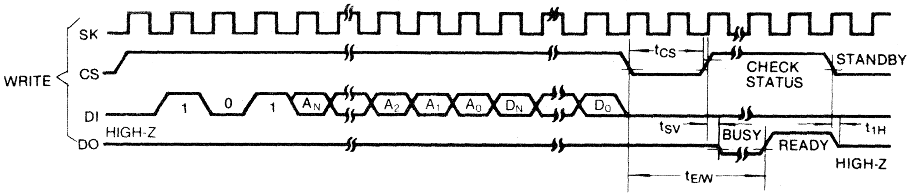
ORGANIZATION

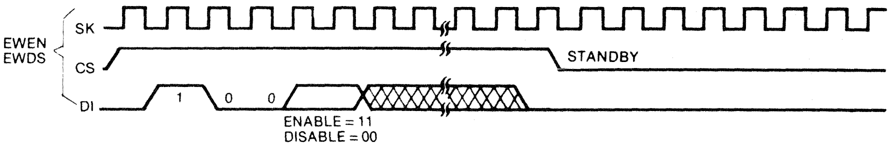
P/N	Organization	AN	DN
KM93C67V	512× 8	A_8	D_7
	256×16	A_7	D_{15}
KM93C57V	256× 8	A_7	D_7
	128×16	A_6	D_{15}

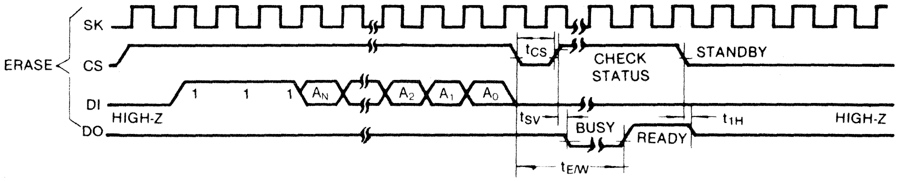
TIMING DIAGRAMS (Continued)

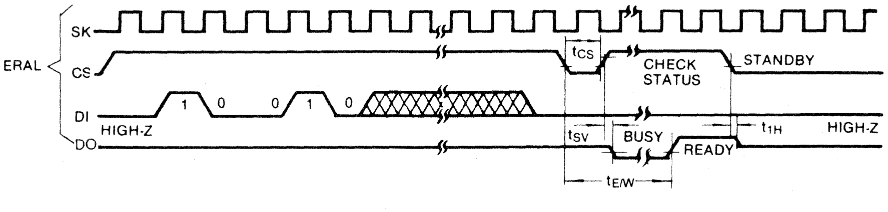
INSTRUCTION TIMING

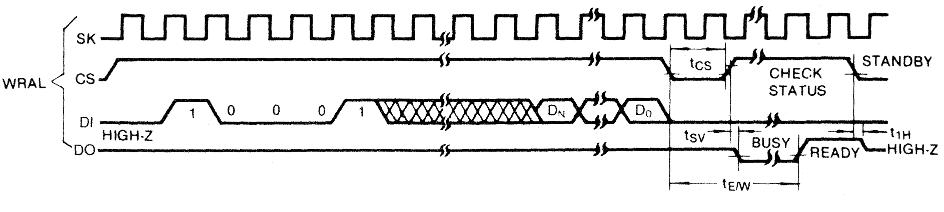












INTRODUCTION

The KM93C57V/67V is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a 2.0V to 4.5V single power supply. The write cycle of the KM93C57V/67V is self timed with the ready/$\overline{\text{busy}}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

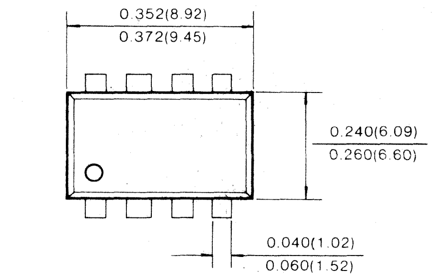
ERAL

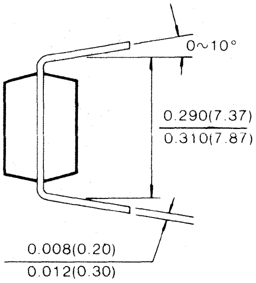
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

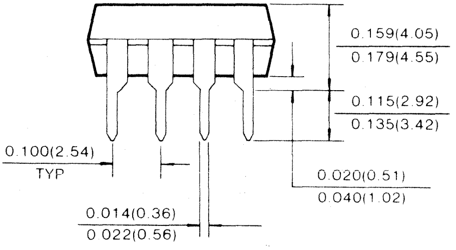
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

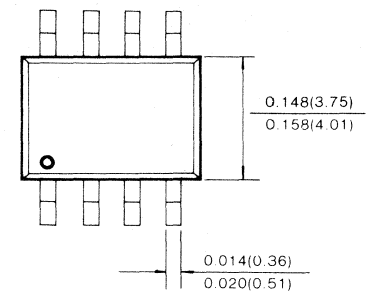
unit; inches (millimeters)

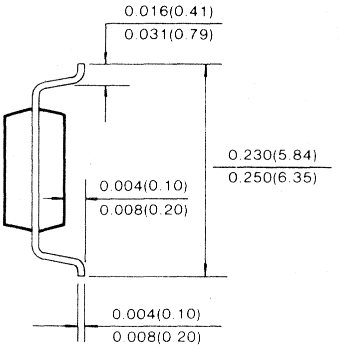


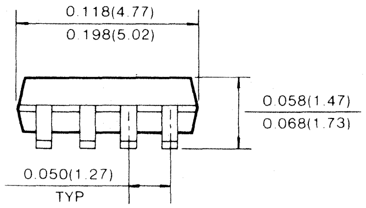




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Write protection with memory pointer**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 100 μA (TTL)**
- **Memory organization:**
  - **— 256 × 16 bits for KM93CS66**
  - **— 128 × 16 bits for KM93CS56**
- **System Clock Frequency: 1 MHz (max.)**
- **Self timed write cycle**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**

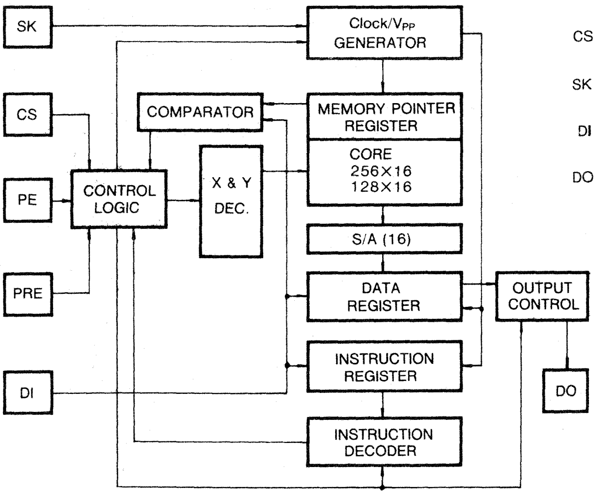
GENERAL DESCRIPTION

The KM93CS56/66 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

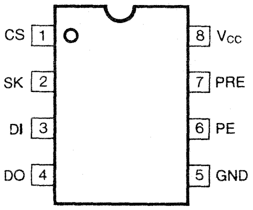
The KM93CS56/66 can be organized as 128/256 registers of 16 bits each, which can be read/written serially and provides data security feature with the memory pointer against the data modification. Besides, this memory pointer address can be locked permanetly.

The KM93CS56/66 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

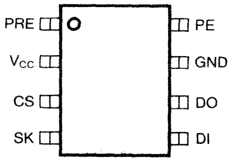
FUNCTIONAL BLOCK DIAGRAM



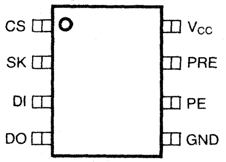
PIN CONFIGURATION



KM93CS56/66



KM93CS56G/66G
(S56/66)



KM93CS56GD/66GD
(S56D/66D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V$_{CC}$	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	100	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	50	μA
Input Low Voltage Levels		V_{IL}		—	0.8	V
Input High Voltage Levels		V_{IH}		2.0	—	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	—	10	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	—	10	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

AC OPERATING CHARACTERISTICS

(V_{CC}=4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
PRE Setup Time	t_{PRES}	Relative to SK	50	—	ns
PE Setup Time	t_{PES}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
PE Hold Time	t_{PEH}	Relative to CS	250	—	ns
PRE Hold Time	t_{PREH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in Tri-state	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

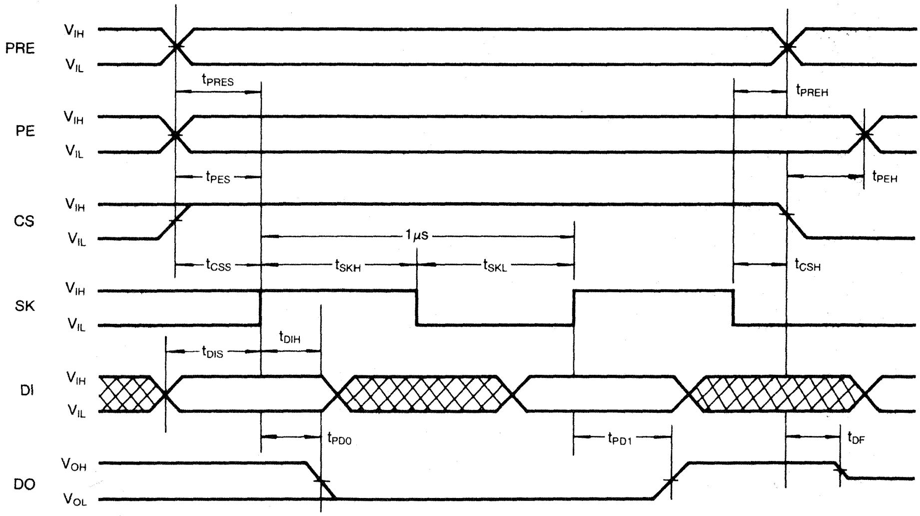
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	PRE	PE	Comment
READ	1	10	A7 - A0	D_{OUT}	0	X	Read register starting at specified address
WRITE	1	01	A7 - A0	D_{15}-D_0	0	1	Write data at memory
EWEN	1	00	11XXXXXX	—	0	1	Erase/Write enable
EWDS	1	00	00XXXXXX	—	0	X	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	0	1	Write all registers
MPRRD	1	10	XXXXXXXX	D_{OUT}	1	X	Read MPR*[1]
MPREN	1	00	11XXXXXX	—	1	1	Enable MPR write related instructions
MPRCLR	1	11	11111111	—	1	1	Clear the MPR
MPRWRT	1	01	A7 - A0	—	1	1	Write address in MPR*
MPRDS	1	00	00000000	—	1	1	One time only instruction to lock the MPR address permanently

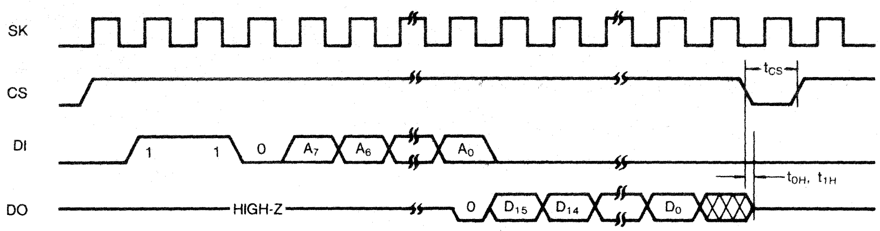
Note: 1. MPR: Memory Pointer Register
2. A7 is a "don't care" address for KM93CS56

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

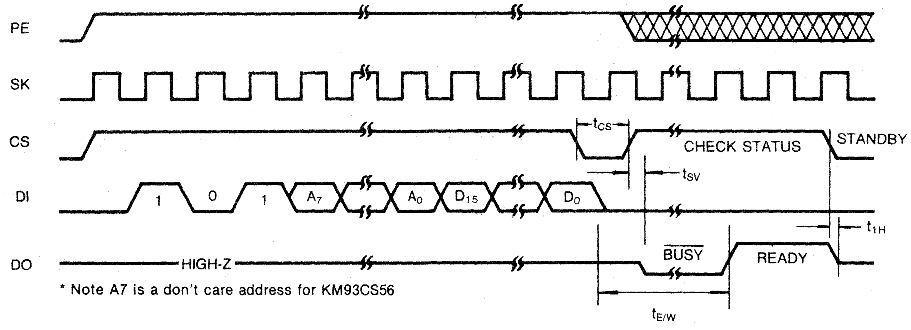


READ (PRE=V_{IL}, PE="Don't Care")



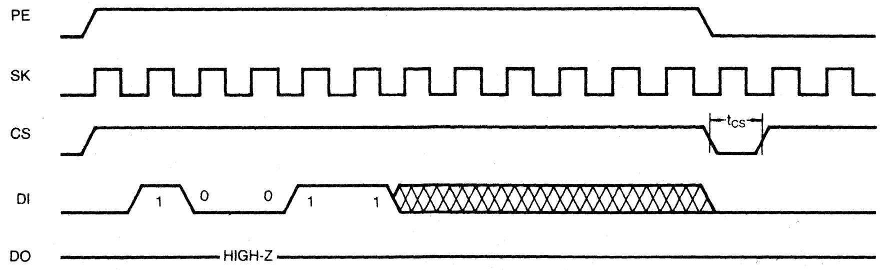
* Note A7 is a don't care address for KM93CS56

WRITE (PRE=V_{IL})

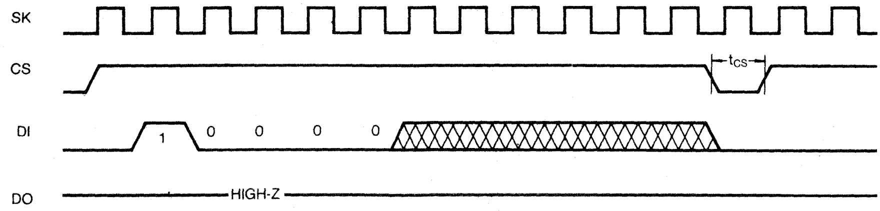


* Note A7 is a don't care address for KM93CS56

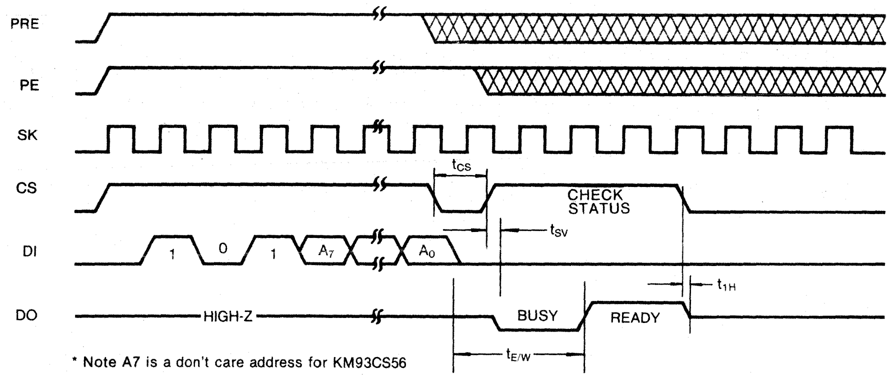
EWEN (PRE=V_{IL})



EWDS (PRE=V_{IL}, PE="Don't Care")

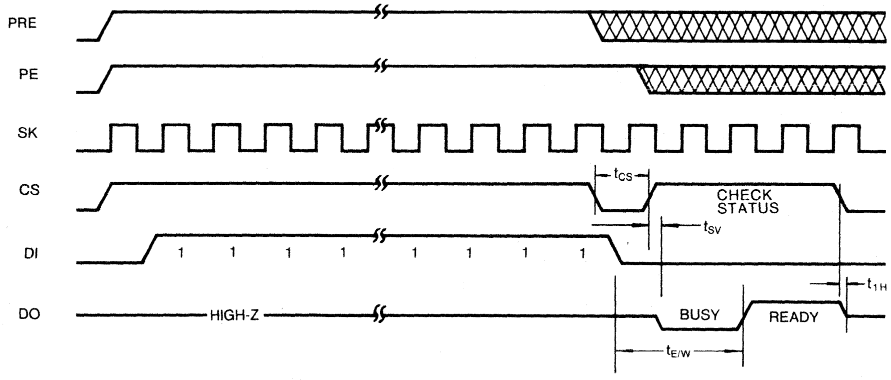


MPRWRT

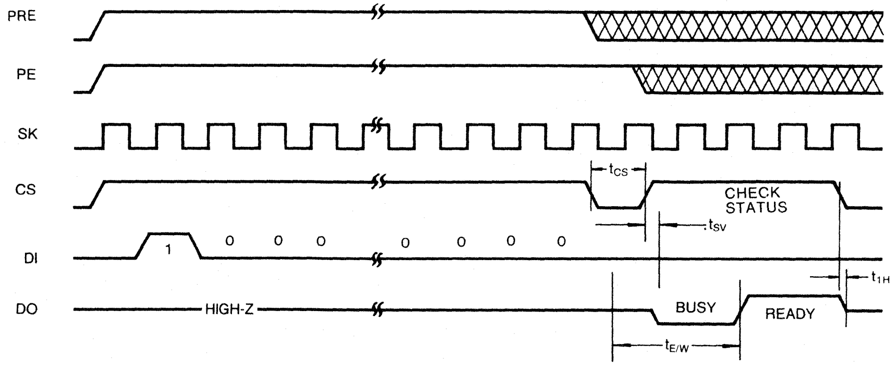


* Note A7 is a don't care address for KM93CS56

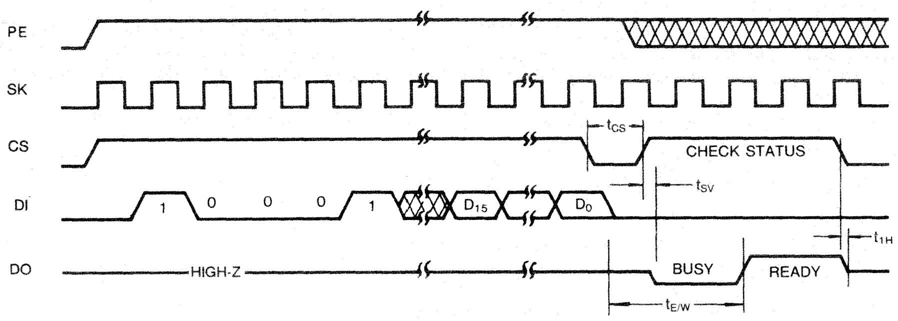
MPRCLR



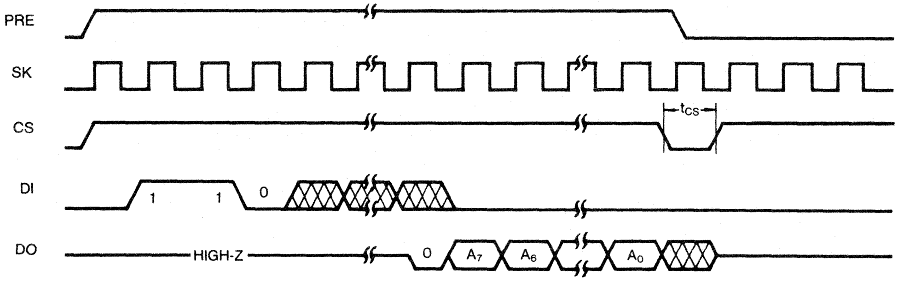
MPRDS



WRAL (PRE=V_{IL})

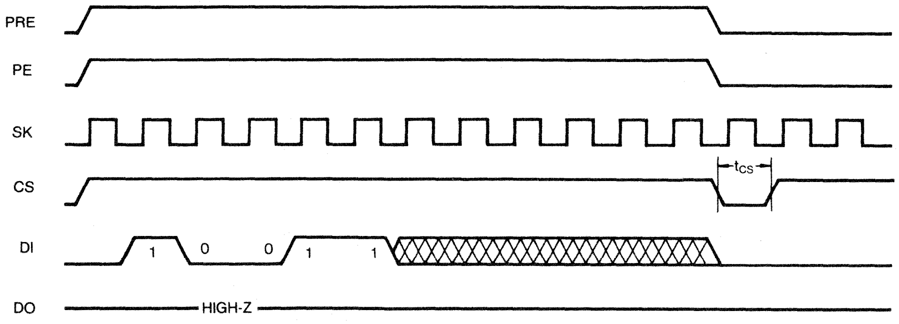


MPRRD (PE="Don't Care")



* Note A7 is a don't care address for KM93CS56

MPREN



INTRODUCTION

The KM93CS56/66 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93CS56/66 is self timed with the ready/busy status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/busy indication period to eliminate bus contention. The KM93CS56/66 offers a data security feature with memory pointer to prevent the protected memory register. Once defined the memory pointer, the memory register is divided into a read/write area and read only area. The addresses equal to or greater than the memory pointer are protected from the Write operation unless clearing the memory pointer register.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string. After 16 bits are clocked out, the device read out the next address automatically. To terminate the read operation CS pin must be toggled high to low.

EWEN/EWDS

The KM93CS56/66 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/busy status is indicated at the DO pin by bringing CS high during write cycle. During loading the WRITE instruction, the PE pin must be high, however after loading the WRITE instruction, the PE pin becomes "don't care".

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are writen simultaneously with given data. The WRAL instruction is valid only when the memory pointer register has been cleared by executing a MPRCLR instruction and while loading the WRAL instruction, the PE pin must be held high, however after loading the WRAL instruction, the PE pin becomes "don't care"

MPRRD

The memory pointer register read (MPRRD) instruction outputs serial 8-bit address stored in the memory pointer register on the DO pin. Like the read operation, a dummy bit (logical "0") precedes the 8 bit address string. While loading the MPRRD instruction, PRE pin must be held high.

MPREN

The memory pointer register enable (MPREN) instruction is used to enable the MPRCLR. MPRWRT and MPRDS modes. The device must be in EWEN mode, before MPREN mode is executed. Both the PRE and PE pin must be held high while loading the MPREN instruction, however after loading the instruction, PE and PRE pins become "don't care". Note that MPREN instruction must be immediately preceded before executing a MPRCLR, MPRWRT, or MPRDS instruction.

MPRCLR

The memory pointer clear (MPRCLR) instruction reset the address stored in the memory pointer register. After executing the MPRCLR, the entire memory register can be programmed by using WRITE and WRAL instruction. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care".

MPRWRT

The memory pointer register write (MPRWRT) instruction program the memory pointer address into the memory pointer register. Once defined the memory pointer address, the memory registers, which has greater than or equal to the memory pointer address, are protected from the data modification. The memory pointer register must be reset before moving the memory pointer address, by executing the MPRCLR instruction. Both the PRE and PE pin must be held high while loading the MPWRT instruction. Once enabled this instruction, both the PE and PRE pins become "don't care"

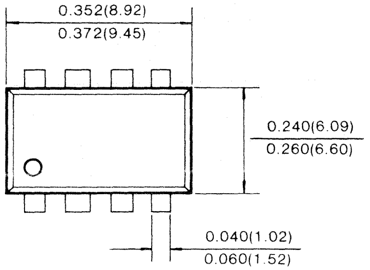
MPRDS

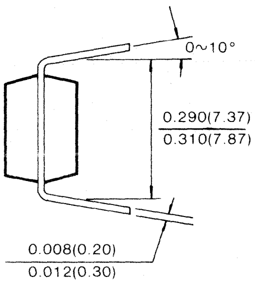
The memory pointer function disable (MPRDS) instruction is one time only instruction. The MPRWRT, MPRCLR, and MPREN instruction is disabled by executing this instruction. Therefore the address of the memory pointer register is permanently unalterable so that the memory registers whose address is greater than or equal to the memory pointer address, are not afford to modify the data permanetly. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care."

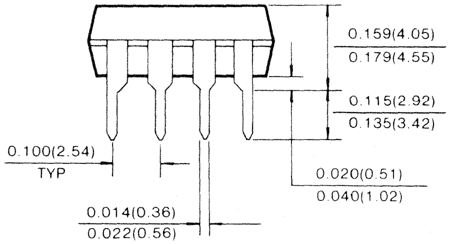
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

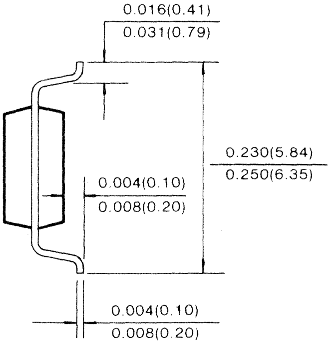
unit: inches (millimeters)

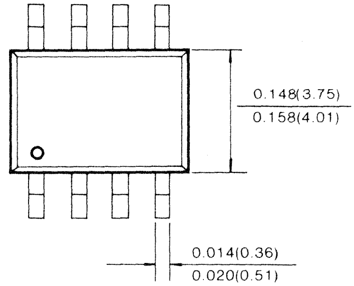


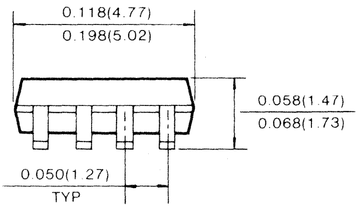




8 PIN PLASTIC SMALL OUT LINE PACKAGE







KM28C16/KM28C17 CMOS EEPROM

2K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C16/KM28C17: Commercial**
  - **— KM28C16I/KM28C17I: Industrial**
- **Simple Byte Write**
  - **— Single TTL Level Write Signal**
  - **— Latched Address and Data**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
  - **— Ready/$\overline{\text{Busy}}$ Output Pin (KM28C17)**
  - **— $\overline{\text{Data}}$-Polling and Verification**
- **32-byte page Write 2ms**
  - **— Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **100,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

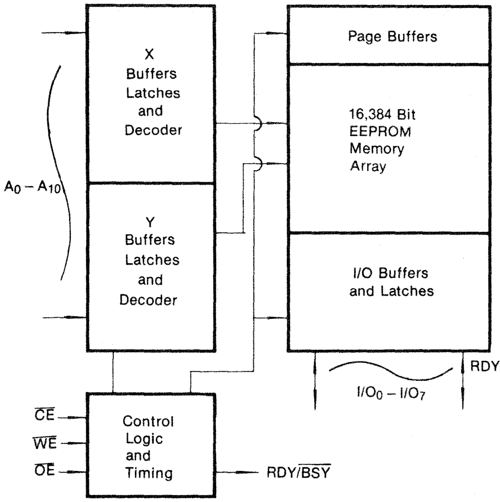
The KM28C16/C17 is a 2,048 x 8 bit Electrically Erasable Programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C16/C17 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 2ms write period. A 32-byte page write enables an entire chip written in 128ms.

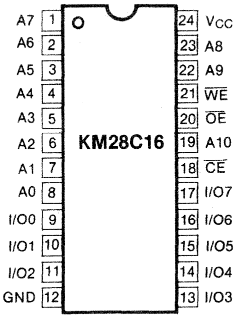
The KM28C16/C17 features $\overline{\text{Data}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM28C17 features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

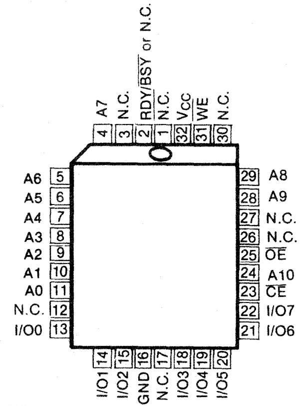
The KM28C16/C17 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

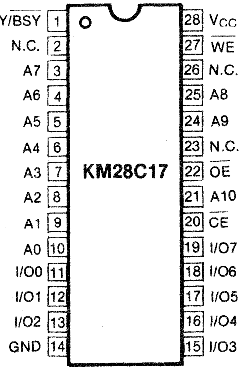
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION







Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{\text{Busy}}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C16/C17: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C16I/C17I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{\text{DATA}}$-Polling	$I/O_7 = \overline{D}_7$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C16/C17: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C16I/C17I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C16-15 KM28C17-15		KM28C16-20 KM28C16I-20 KM28C17-20 KM28C17I-20		KM28C16-25 KM28C16I-25 KM28C17-25 KM28C17I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

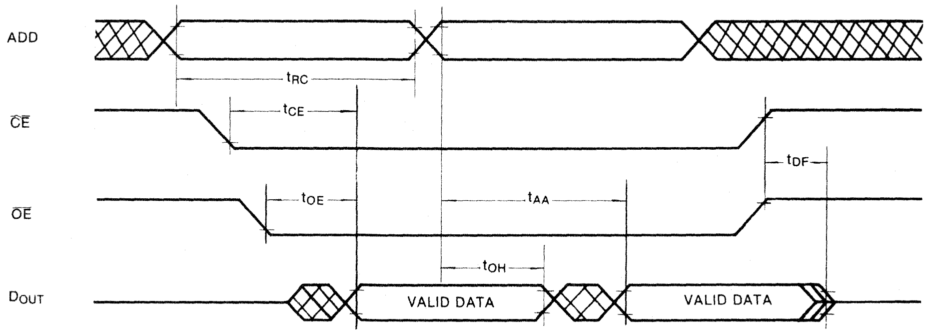
WRITE CYCLE

Parameter		Symbol	Min	Max	Unit
Write Cycle Time	Commercial Industrial	t_{WC}	2 5		ms ms
Address Set-Up Time		t_{AS}	0		ns
Address Hold Time		t_{AH}	80		ns
Write Set-Up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
$\overline{CE}$ Pulse Width		t_{CW}	100		ns
Output Enable Set-Up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
$\overline{WE}$ Pulse Width		t_{WP}	100		ns
Data Set-Up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns
Time to Device Busy		t_{DB}		100	ns
Busy to Write Recovery Time		t_{BWR}	50		ns
Byte Load Cycle Time		t_{BLC}	0.2	100	μs
Last Byte Loaded to $\overline{Data}$ Polling		t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at a rising edge of $\overline{WE}$.

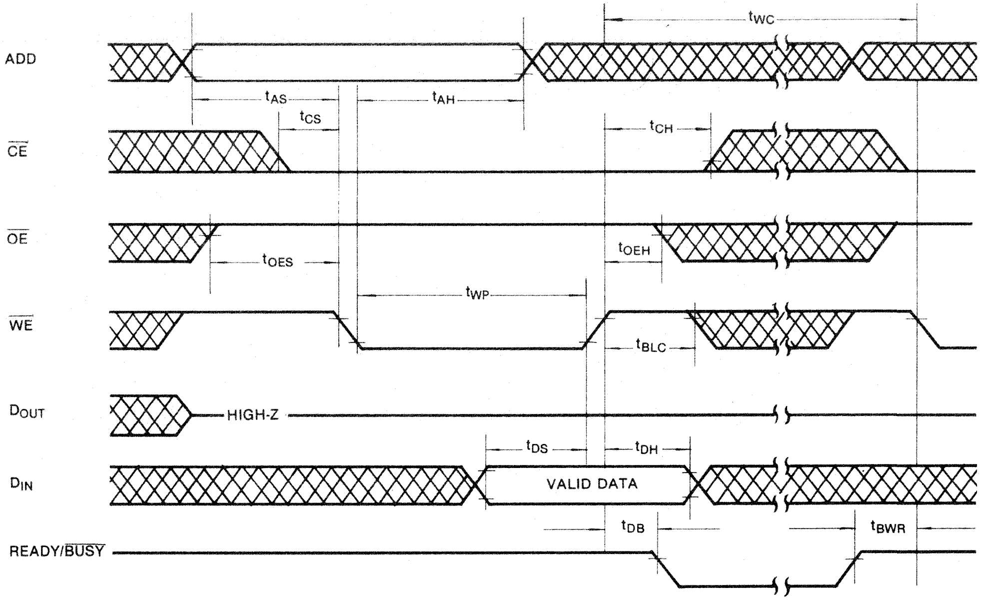
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

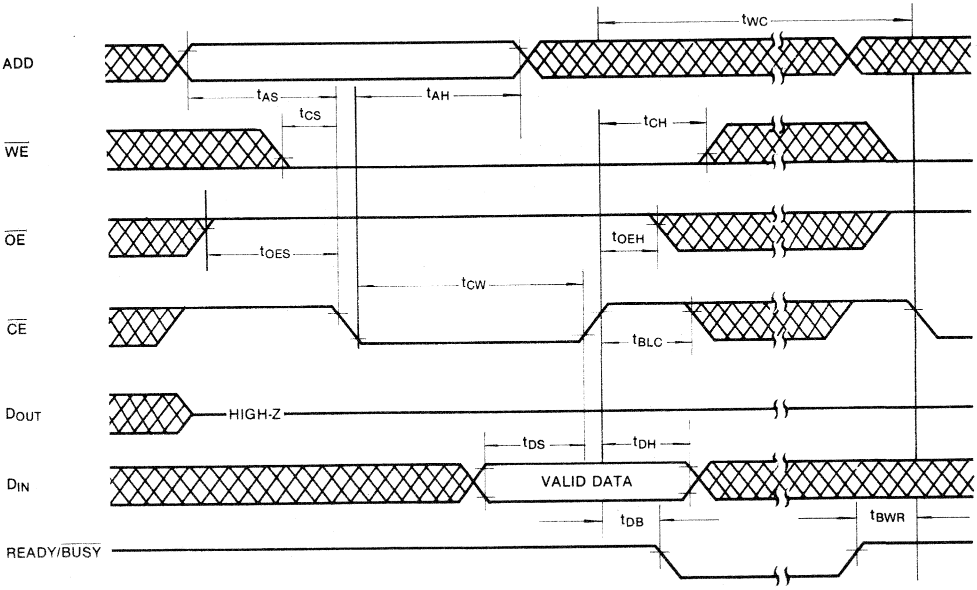


TIMING DIAGRAMS (Continued)

WE CONTROLLED WRITE CYCLE

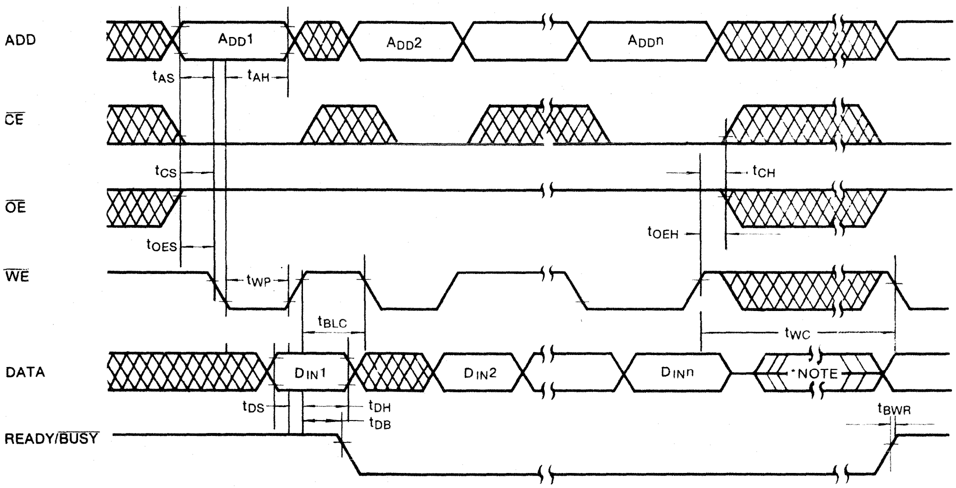


CE CONTROLLED WRITE

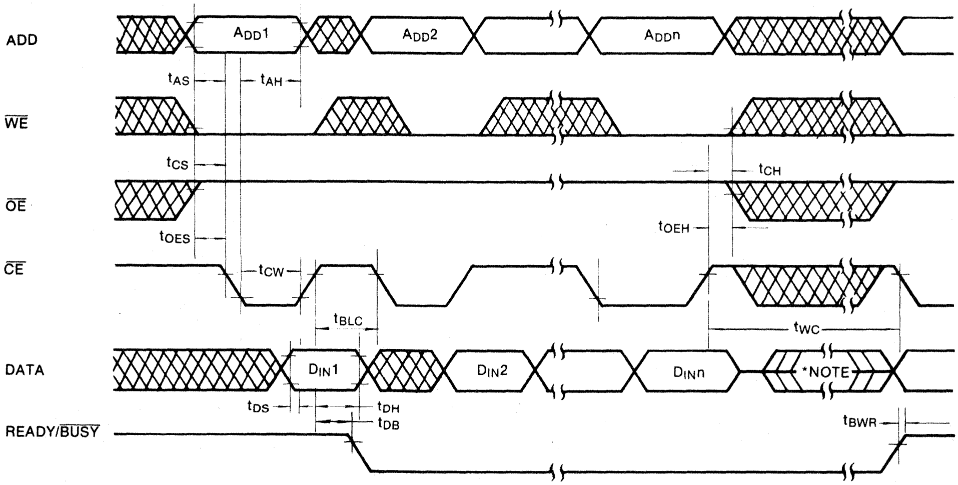


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $\overline{D_{IN}n}$ when the chip is read.
I/O_0-I/O_6 have high impedance.

DEVICE OPERATION

READ

Reading data from the KM28C16/C17 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C16/C17 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C16/C17 is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM28C16/C17.

**** PAGE WRITE MODE ****

The KM28C16/C17 allows up to 32 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 bytes of data are loaded into the KM28C16/C17 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C16/C17 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_4) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A_5-A_{10}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C16/C17 also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C16/C17 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C16/C17 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise, the width shorter than 20ns (typ.) will not start any unwanted write cycle.

Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.0$ volts, the write inhibits V_{CC} level.

During power-up, the KM28C16/C17 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

DATA POLLING

The KM28C16/C17 features $\overline{\text{Data}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_7, an inverted value of the last data loaded in to the EEPROM (I/O_0-I/O_6 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION (Continued)

READY/$\overline{\text{BUSY}}$

The KM28C17 has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/$\overline{\text{Busy}}$ output is configured as an open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ outputs to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready/$\overline{\text{Busy}}$ pin.

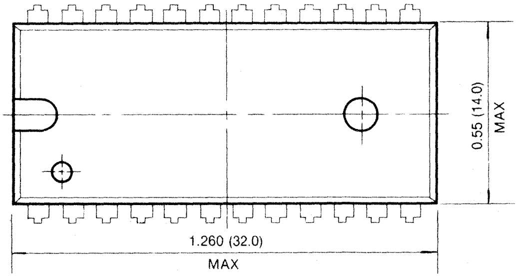
ENDURANCE AND DATA RETENTION

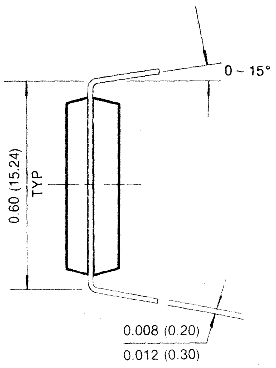
KM28C16/C17 is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation, and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

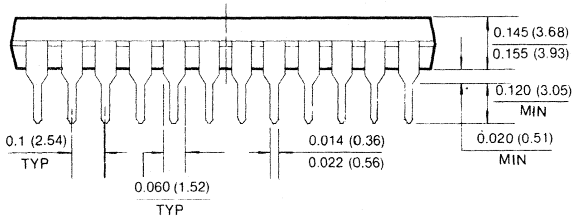
PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



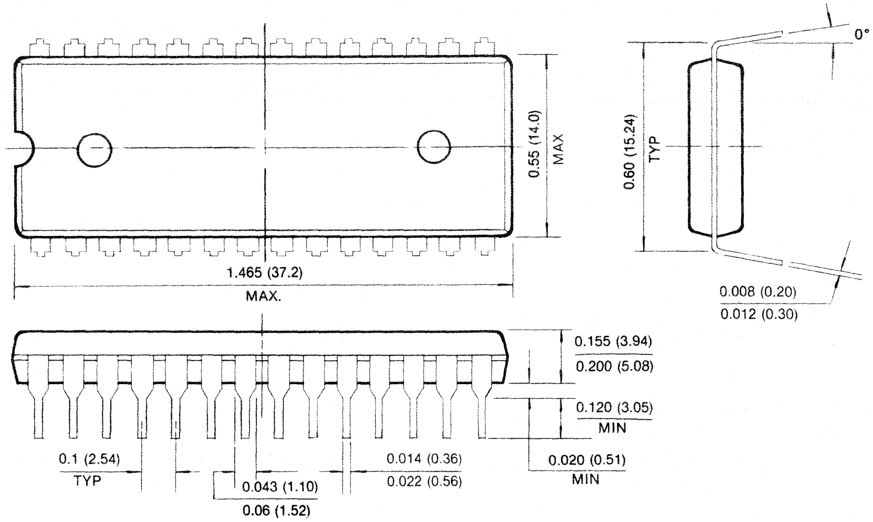




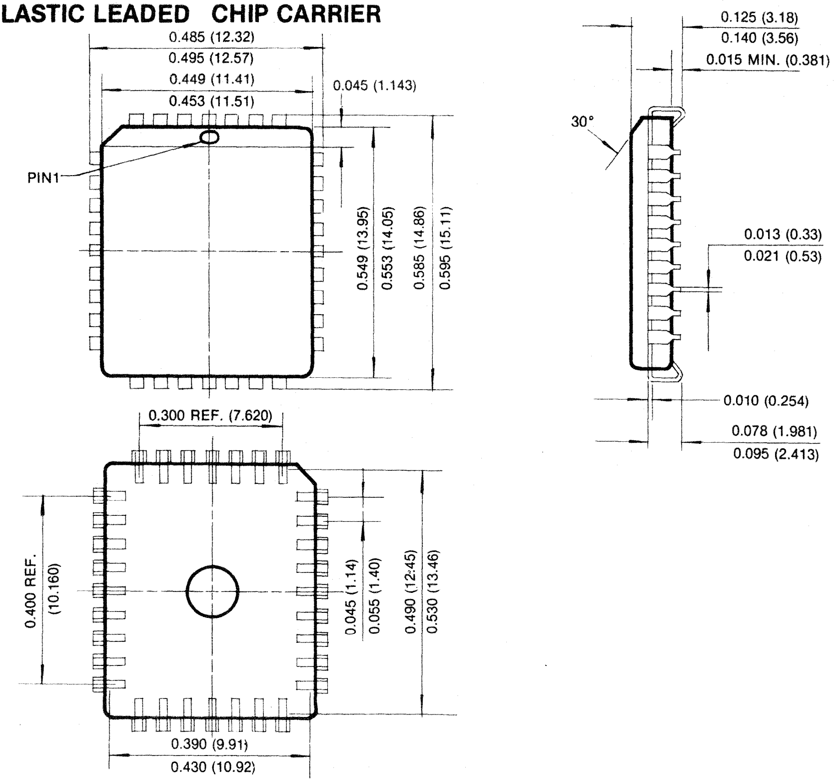
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



8K×8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C64A/65A: Commercial**
  - **— KM28C64AI/65AI: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Internal Erase-Before-Write**
  - **— Ready/Busy Output Pin (KM28C65A)**
- **Fast Write Cycle Time**
  - **— 64-Byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 0.7 seconds**
- **Data-Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating-Gate Technology**
  - **— Endurance: 100,000 Cycle**
  - **— Data Retention: 10 years**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

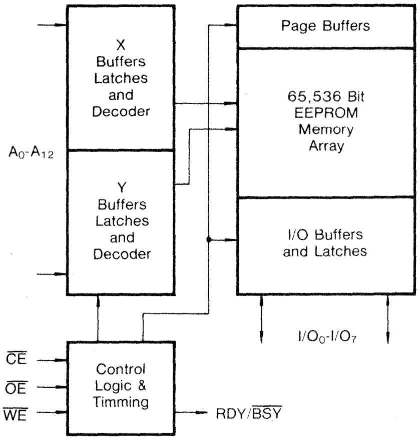
The KM28C64A/65A is a 8,192×8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C64A/65A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 0.7 seconds.

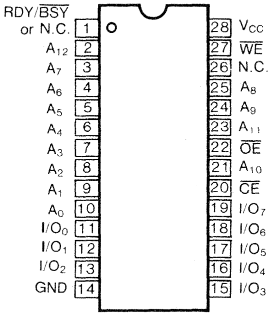
The KM28C64A/65A also features Data-polling and a Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware. The KM28C65A features Read/Busy which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

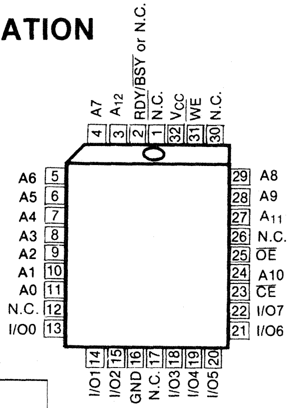
The KM28C64A/65A is designed for applications up to 100,000 write cycles per byte. It's on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION





Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
RDY/BSY	Ready/Busy Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C64A/65A : Voltage reference to V_{SS}, T_A=0°C to +70°C
KM28C64AI/65AI : Voltage reference to V_{SS}, T_A=−40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, all I/O's open (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}-0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

Note 1: All address toggling from V_{IL} to V_{IH} at 8.4MHz.

CAPACITANCE (T_A=25°C, f=1.0 MHz))

Item	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{\text{Data}}$ Polling	$I/O_7=\overline{D}_7$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C64A/65A : $T_A=0°C$ to $+70°C$ $V_{CC}=5V\pm10\%$, unless otherwise noted
KM28C64AI/65AI: $T_A=-40°C$ to $+85°C$ $V_{CC}=5V\pm10\%$, unless otherwise noted

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L=100pF$

READ CYCLE

Parameter	Symbol	KM28C64A-12 KM28C65A-12		KM28C64A-15 KM28C64AI-15 KM28C65A-15 KM28C65AI-15		KM28C64A-20 KM28C64AI-20 KM28C65A-20 KM28C65AI-20		KM28C64A-25 KM28C64AI-25 KM28C65A-25 KM28C65AI-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		250		ns
Chip Enable Access Time	t_{CE}		120		150		200		250	ns
Address Access Time	t_{AA}		120		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

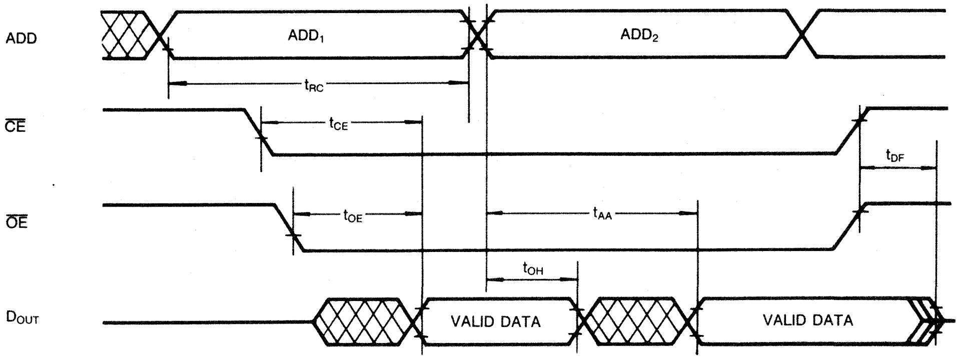
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at rising edge of $\overline{WE}$.

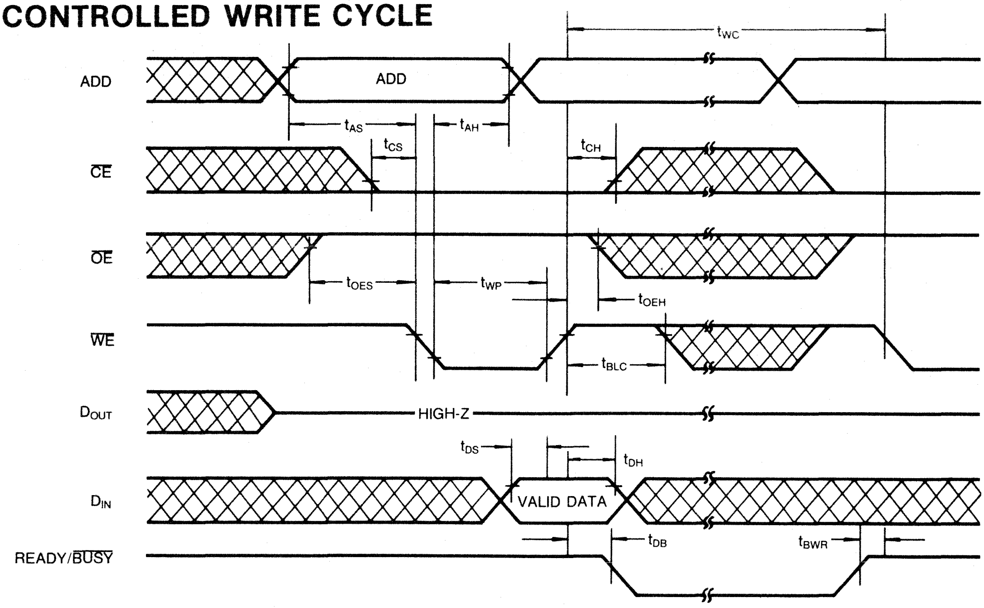
TIMING DIAGRAM

READ CYCLE ($\overline{WE}=V_{IH}$)

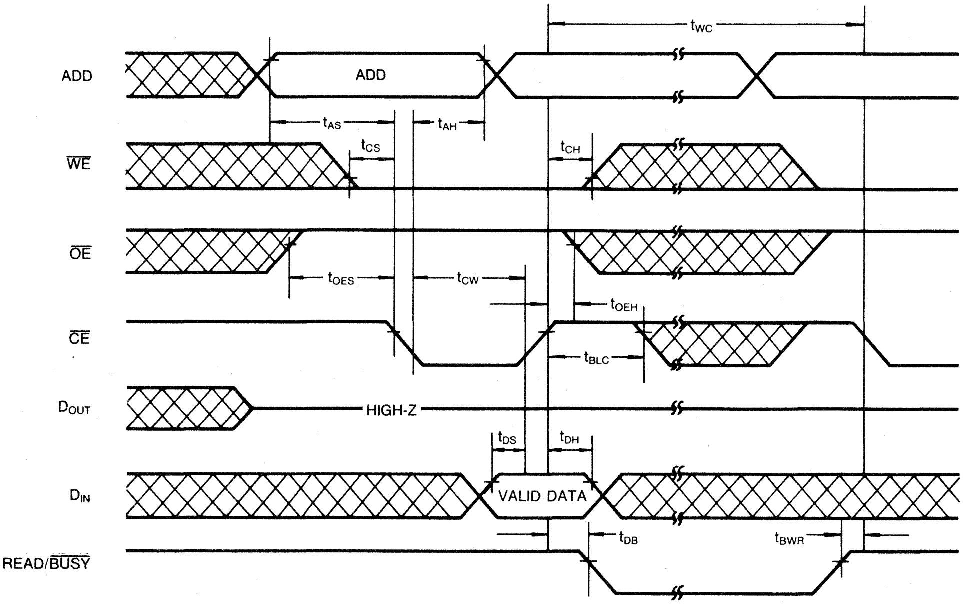


TIMING DIAGRAM (Continued)

WE CONTROLLED WRITE CYCLE

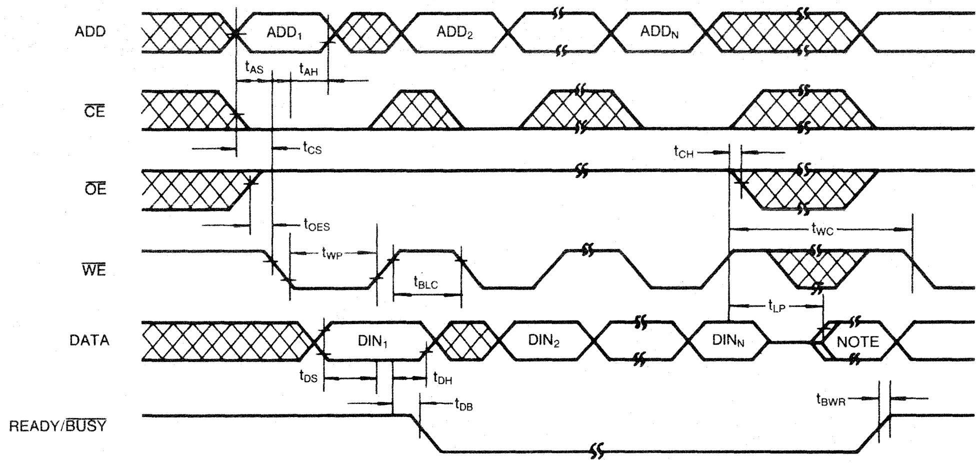


CE CONTROLLED WRITE CYCLE

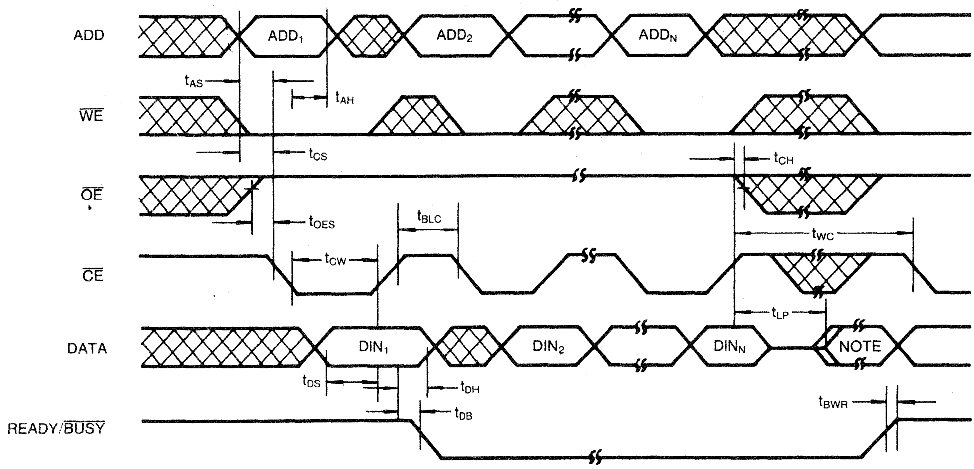


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE (WE CONTROLLED WRITE CYCLE)



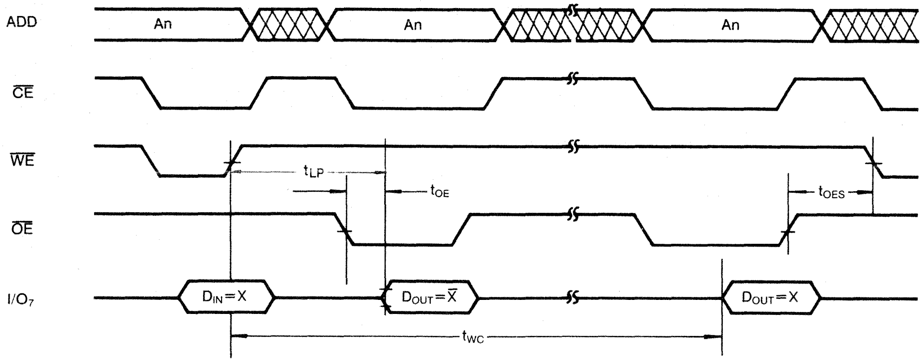
PAGE MODE WRITE (CE CONTROLLED WRITE CYCLE)



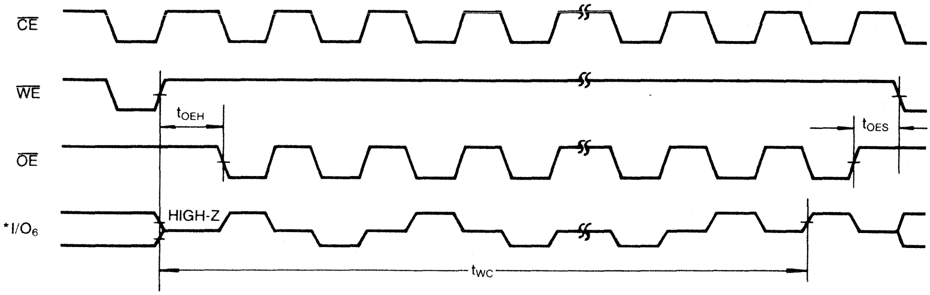
* NOTE: I/O₇ output $\overline{\text{DIN}_N}$ when the chip is read.
I/O₆ is toggling between "1" and "0" when the chip is successively read.

TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



TOGGLE BIT CYCLE



* During the write cycle, I/O_6 will toggle between "1" and "0".

DEVICE OPERATION

READ

Reading data from the KM28C64A/65A is similar to reading data from a SRAM. A read cycle occurs when $\overline{\text{WE}}$ is high and $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low. If either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The DATA I/O pins are in the high impedance state whenever $\overline{\text{OE}}$ or $\overline{\text{CE}}$ is high.

WRITE

Writing data into the KM28C64A/65A is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64A/65A is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolitile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C64A/65A allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C64A/65A internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C64A/65A by sequentially pulsing $\overline{\text{WE}}$ with $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ high. For each addressed location in the page, address is latched on the falling edge of the $\overline{\text{WE}}$ and data is latched on the rising edge of the $\overline{\text{WE}}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for the data loading (t_{BLC}) is reset at the falling edge of $\overline{\text{WE}}$ and starts at every rising edge of $\overline{\text{WE}}$, the only requirement on $\overline{\text{WE}}$ to continue loding the data is that the interval between $\overline{\text{WE}}$ pulses dose not exceed the maximum t_{BLC} (150μs). If $\overline{\text{OE}}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{\text{WE}}$ signal is blocked by $\overline{\text{OE}}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{\text{WE}}$ pulse if $\overline{\text{OE}}$ is low. The nonvolatile write starts if $\overline{\text{WE}}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{\text{WE}}$ low to high transition. The page address for the nonvolatile write is the "X" address (A6-A12) latched on the last $\overline{\text{WE}}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. the new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64A/65A also supports $\overline{\text{CE}}$ controlled write cycle. That means $\overline{\text{CE}}$ can be used to latch address and data as well as $\overline{\text{WE}}$.

STANDBY

Power comsumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{\text{CE}}$. Whenever $\overline{\text{CE}}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{\text{OE}}$ or $\overline{\text{WE}}$.

DATA PROTECTION

Features have been designed into the KM28C64A/65A to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64A/65A has a protection feature against $\overline{\text{WE}}$ noises; a $\overline{\text{WE}}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than $V_{WI}=3.0$ volts, the write inhibits V_{CC} level. During power-up, the KM28C64A/65A automatically prevents any write operation for a period of 5ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{\text{WE}}$ and $\overline{\text{CE}}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{\text{OE}}$ low or $\overline{\text{WE}}$ high or $\overline{\text{CE}}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C64A/65A has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm, followed by a write or page write operation. Once the protection mode is enabled, the KM28C64A/65A will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by exection a SDP disable software algorithm. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

*** $\overline{\text{DATA}}$ POLLING ***

The KM28C64A/65A features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme dose not require any external hardware. During the write period, any attempt to read the EEPROM will produce, at I/O_7, an inverted inverted value of the last data loaded into the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

*** TOGGLE BIT ***

The KM28C64A/65A also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 between "1" and "0". Once the write cycle is complete, the toggling will stop and valid data will be read.

*** READY/$\overline{\text{BUSY}}$ ***

The KM28C65A has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/$\overline{\text{Busy}}$ output is configured as an open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max)-V_{OL}(max)}{I_{OL}+I_L} = \frac{5.1V}{2.1mA+I_L}$$

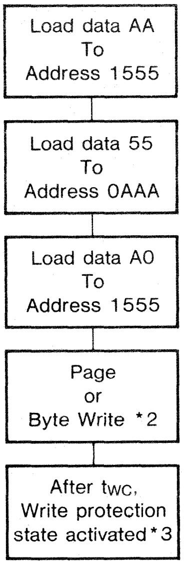
where ΣI_L is the sum of the input currents of all devices tied to the Ready/$\overline{\text{Busy}}$ pin.

ENDURANCE AND DATA RETENTION

KM28C64A/65A is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation. The device also featires an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

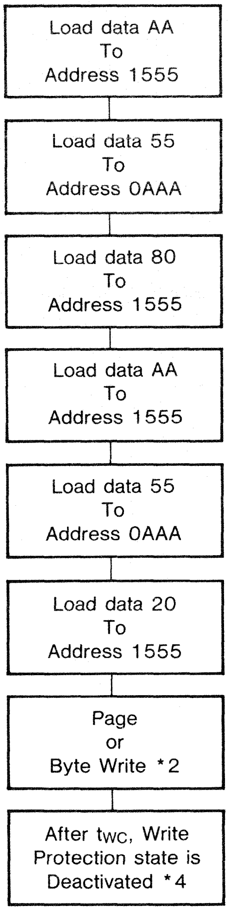
SOFTWARE DATA PROTECTION ALGORITHIM*[1]

SDP Enable Sequence



* Write mode enabled

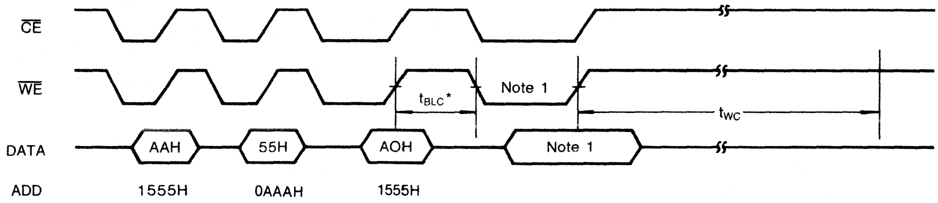
SDP Disable Sequance



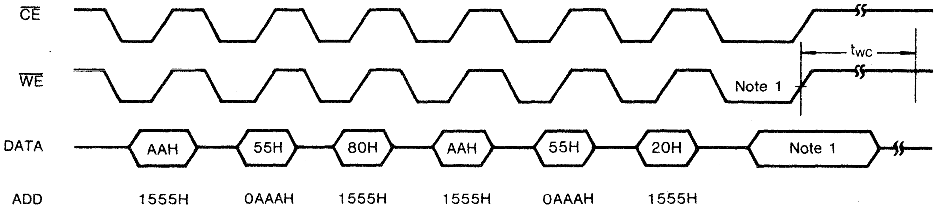
Note: 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{12}-A_0 (HEX)
2. 1 to 64 byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is writtern.
4. Write protection state will be deactived after.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP Enable Timing SEQUENCE



SDP Disable Timing SEQUENCE



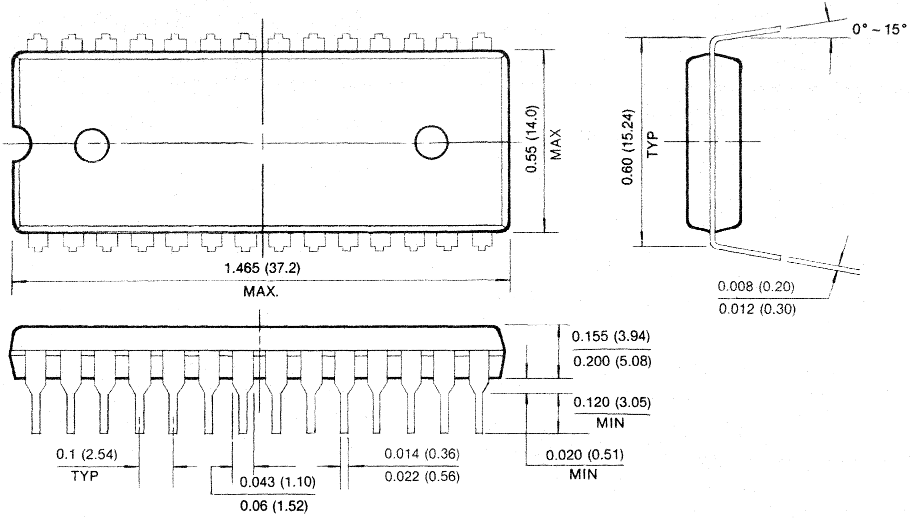
* $\leq t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

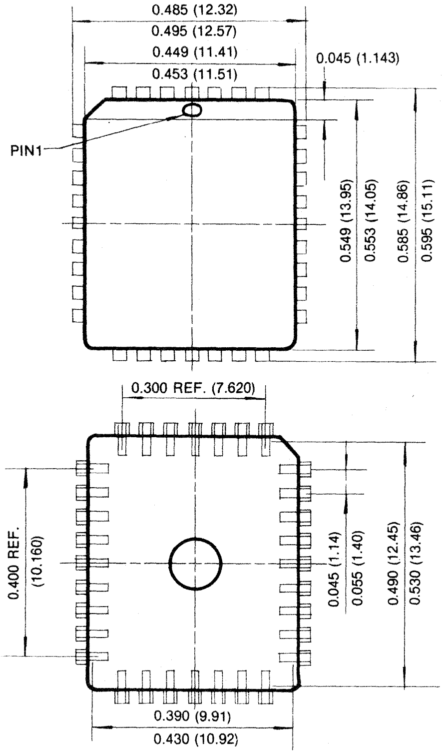
PACKAGE DIMENSIONS (Continued)

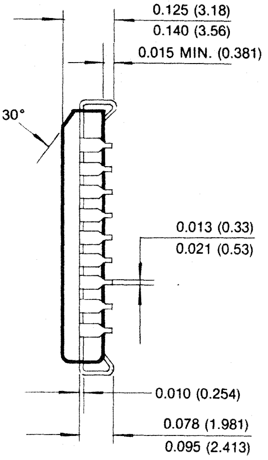
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER





32K×8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C256: Commercial**
  - **— KM28C256I: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
- **Fast Write Cycle Time**
  - **— 64-byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 2.5 seconds**
- **$\overline{\text{Data}}$ Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max.)**
  60mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating—Gate Technology**
  - **— Endurance: 100,000**
  - **— Data Retention: 10 years**
- **JEDEC Approved Byte-Wide Pinout**

GENERAL DESCRIPTION

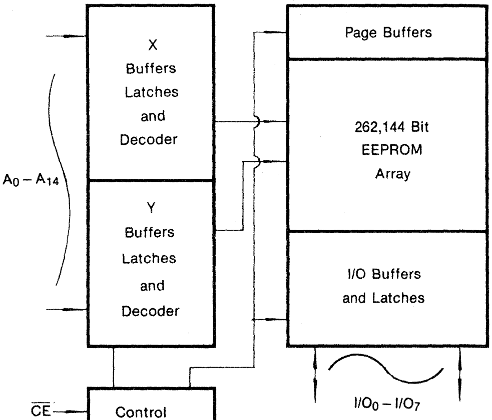
The KM28C256 is a 32,768×8 bit Electrically Erasable Programable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C256 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 2.5 seconds.

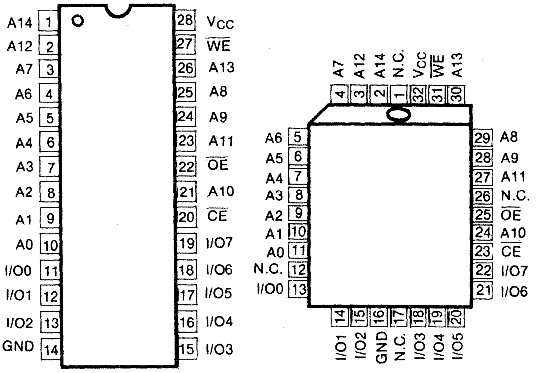
The KM28C256 also features Data polling and Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware.

The KM28C256 is designed for applications up to 100,000 write cycles per byte. Its on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C256: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C256I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open all addresses* (Note 1)	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{Data}$-Polling	$I/O_7 = \overline{D}_7$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C256: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C256I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C256-15 KM28C256I-15		KM28C256-20 KM28C256I-20		KM28C256-25 KM28C256I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

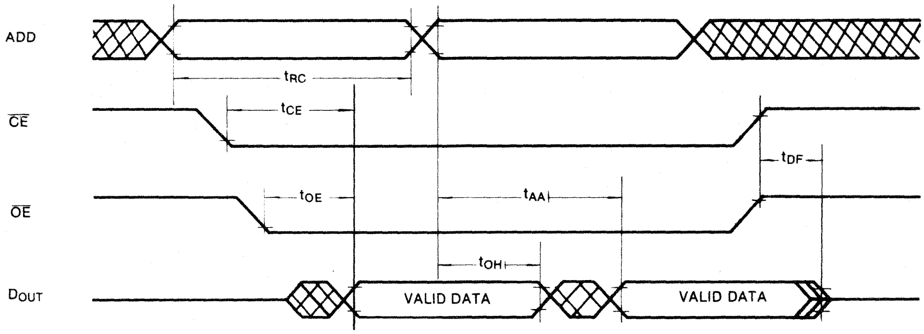
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{\text{CE}}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{\text{WE}}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{\text{Data}}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{\text{WE}}$ and starts at a rising edge of $\overline{\text{WE}}$.

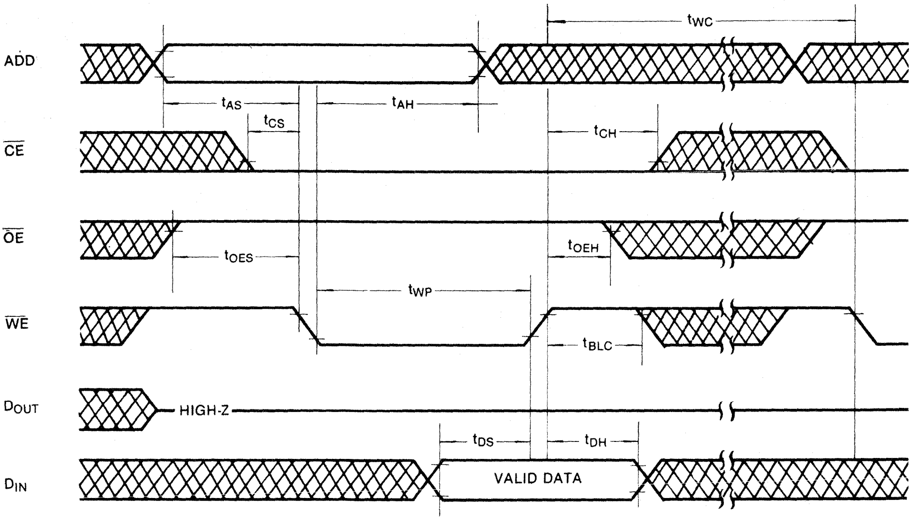
TIMING DIAGRAMS

READ CYCLE $\overline{\text{WE}} = V_{IH}$

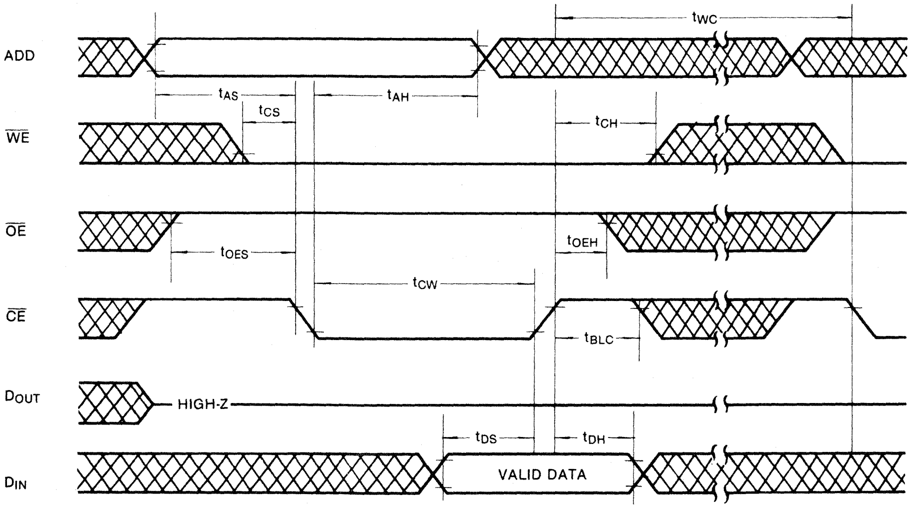


TIMING DIAGRAMS (Continued)

$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE

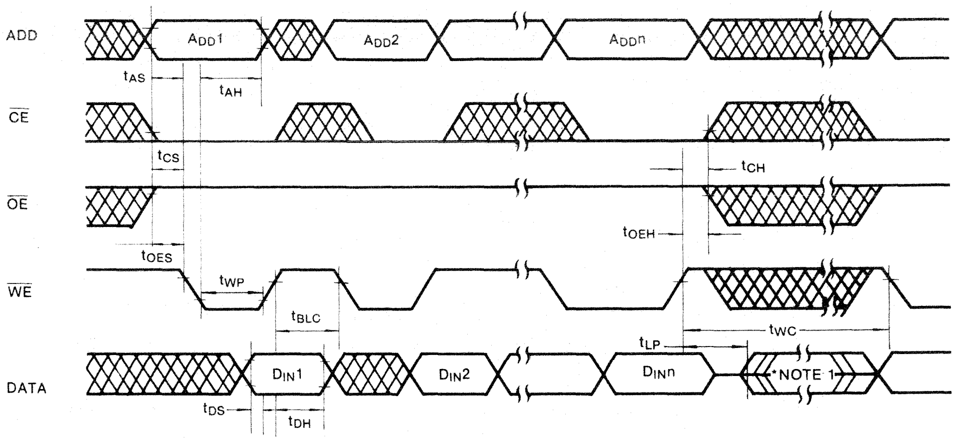


$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE

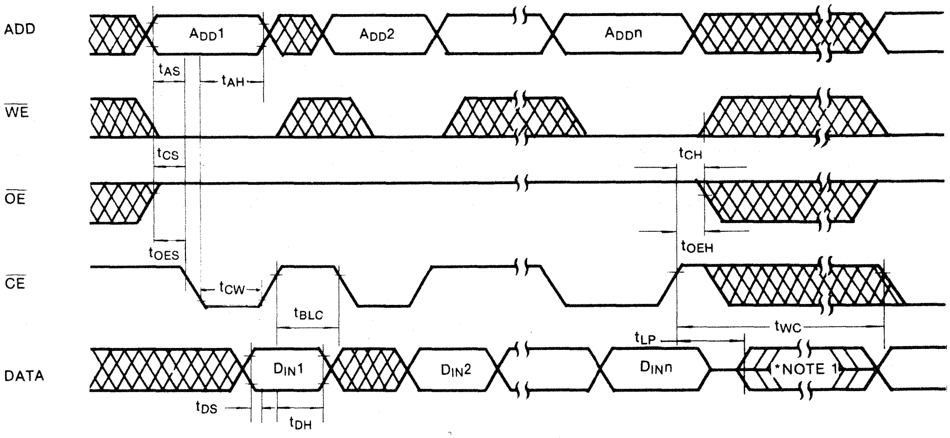


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE (WE CONTROLLED WRITE CYCLE)



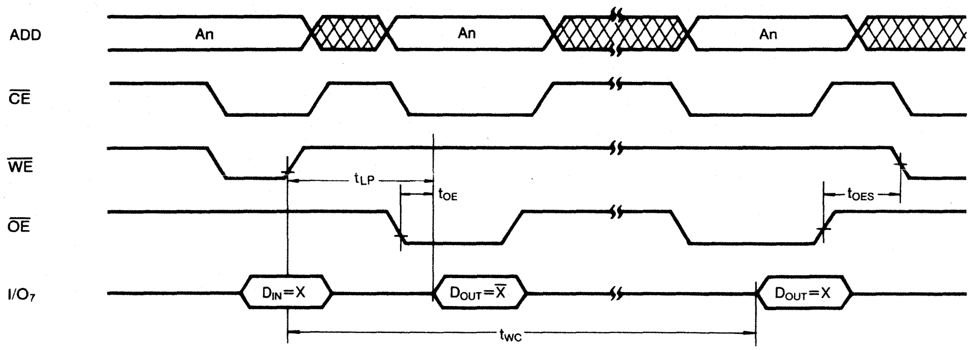
PAGE MODE WRITE (CE CONTROLLED WRITE CYCLE)



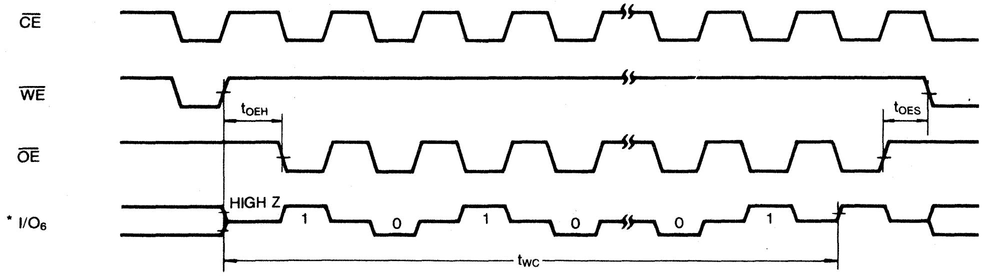
*NOTE 1. I/O$_7$ Outputs $\overline{D_{IN}n}$ when the chip is read.
I/O$_6$ is toggling between "1" and "0" when
the chip is successively read

TIMING DIAGRAMS (Continued)

DATA POLLING CYCLE



TOGGLE BIT CYCLE



*During the write cycle, I/O6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM28C256 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O$_0$-I/O$_7$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

WRITE

Writing data into the KM28C256 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C256 is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C256 allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C256 internal registers and a nonvolatile write period, in which the loaded data in the registers is written to the EEPROM cells of the selected page.

Data is loaded into the KM28C256 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A_6-A_{14}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C256 also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C256 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C256 has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.0$ volts, the write inhibit V_{CC} level. During power-up, the KM28C256 automatically prevents any write operation for a period of 5ms (min.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C256 has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operations if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing a short SDP enable software algorithm, followed by a write operation, either a single byte write or page write operation. Once the protection mode is enabled, the KM28C256 will not write any data if the SDP enable software algorithm is not preceded. The data protection function can be disabled by executing a SDP disable software algorithm. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

**** $\overline{\text{DATA}}$ POLLING ****

The KM28C256 features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read the EEPROM will produce, at I/O_7, an inverted value of the last data loaded into the EEPROM. True data will be produced at all I/O's, once the write cycle has been completed.

**** TOGGLE BIT ****

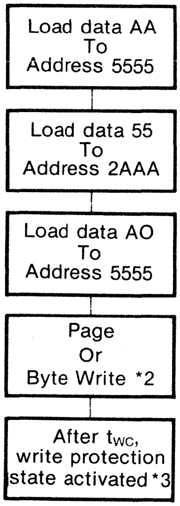
The KM28C256 also provides a toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, successive attempts to read the EEPROM will toggle I/O_6 between '1' and '0'. Once the write cycle is complete, the toggling will stop and valid data will be read.

ENDURANCE AND DATA RETENTION

The KM28C256 is designed for applications requiring up to 100,000 write cycles per byte and ten years of data retention. This means that each byte can be reliably written 100,000 times without degrading device operation. The device also features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

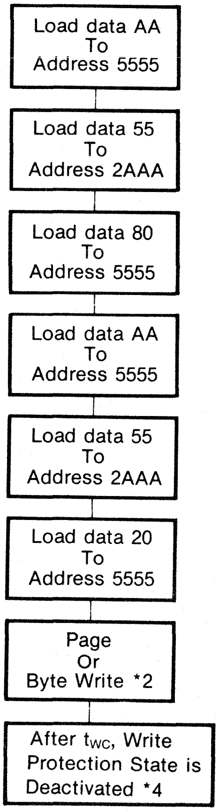
SOFTWARE DATA PROTECTION ALGORITHM*1

SDP Enable Sequence



*Write mode enabled

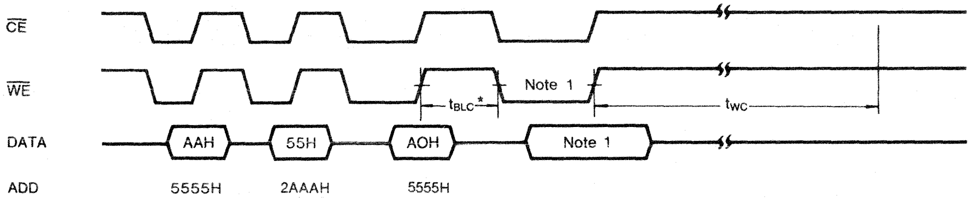
SDP Disable Sequence



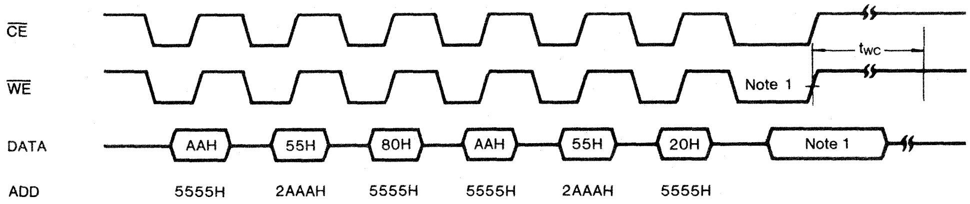
Notes 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{14}-A_0 (HEX)
2. 1 to 64-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is written.
4. Write protection state will be deactivated after t_{WC} even if no data is written.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP Enable Timing SEQUENCE



SDP Disable Timing SEQUENCE

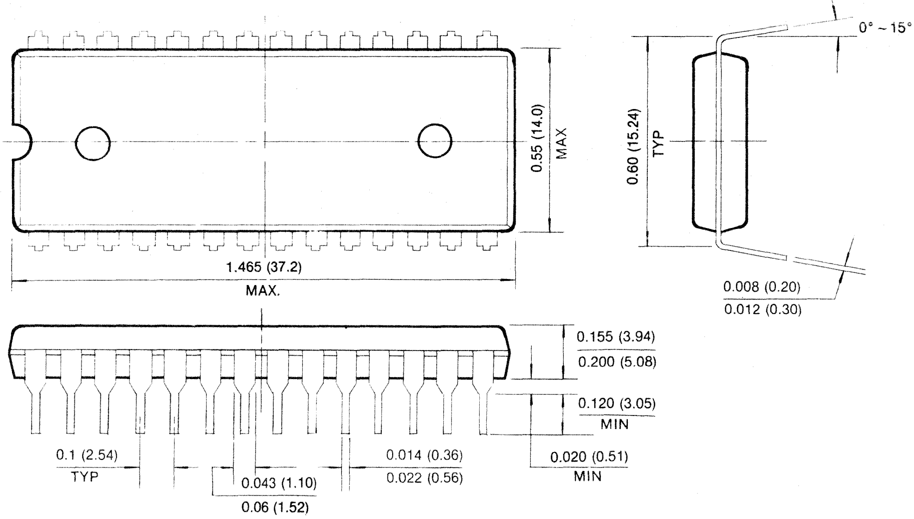


*$\leqslant t_{BLC}$ max.
Note 1 to 64 byte of data may be louded in random order.

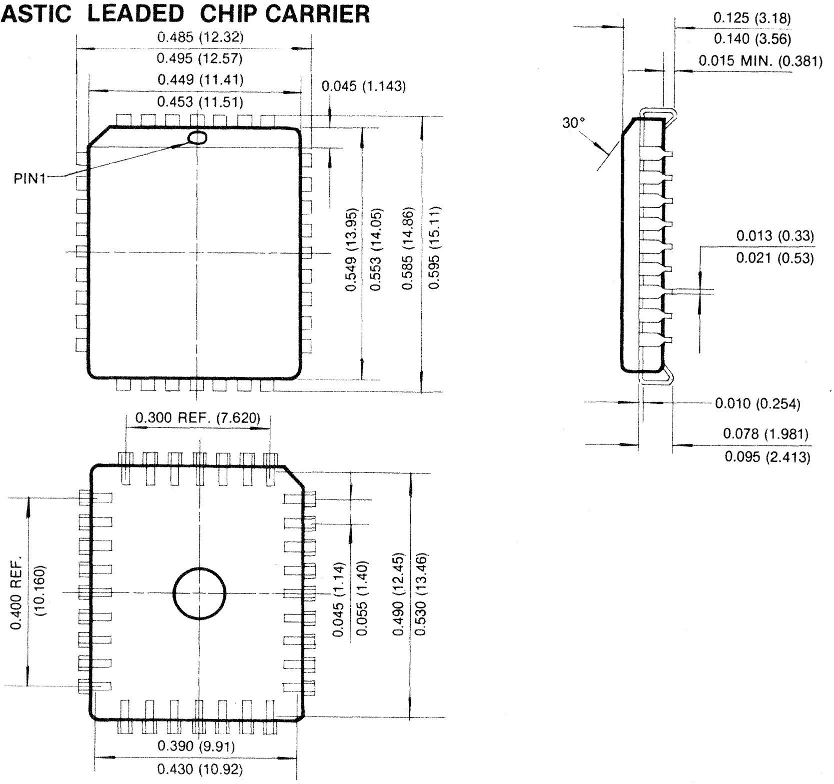
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



32K × 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C256A: Commercial**
  - **— KM28C256AI: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
- **Fast Write Cycle Time**
  - **— 64-byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 2.5 seconds**
- **$\overline{\text{Data}}$ Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 120ns**
- **Power: 100μA—Standby (max.)**
  60mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating—Gate Technology**
  - **— Endurance: 100,000**
  - **— Data Retention: 10 years**
- **JEDEC Approved Byte-Wide Pinout**

GENERAL DESCRIPTION

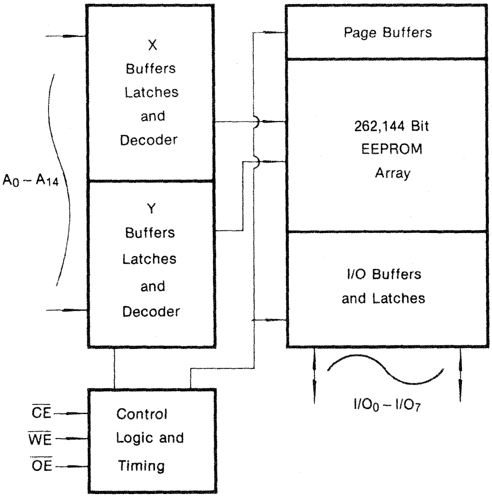
The KM28C256A is a 32,768 × 8 bit Electrically Erasable Programable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C256A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 2.5 seconds.

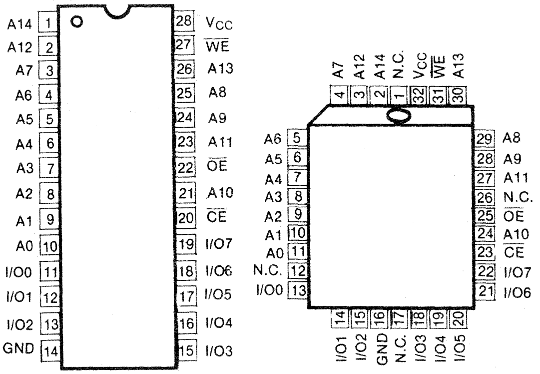
The KM28C256A also features $\overline{\text{Data}}$ polling and Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware.

The KM28C256A is designed for applications up to 100,000 write cycles per byte. Its on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C256A: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C256AI: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open all addresses* (Note 1)	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 8.4MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{\text{Data}}$-Polling	$I/O_7 = \overline{D}_7$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C256A: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C256AI: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C256A-12 KM28C256AI-12		KM28C256A-15 KM28C256AI-15		KM28C256A-20 KM28C256AI-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{CE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		50		60		80	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

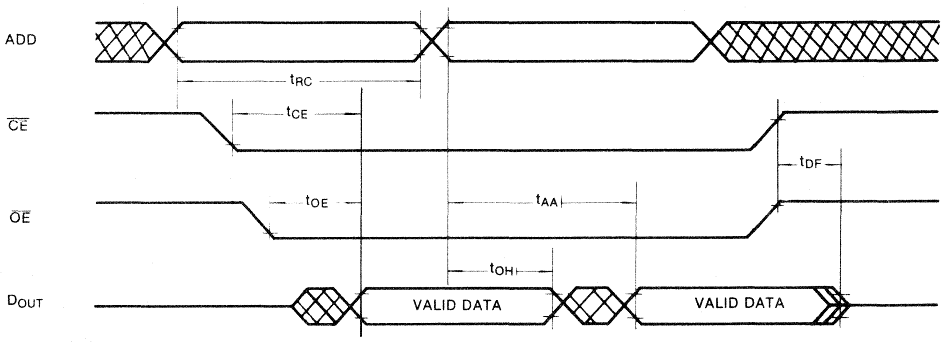
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

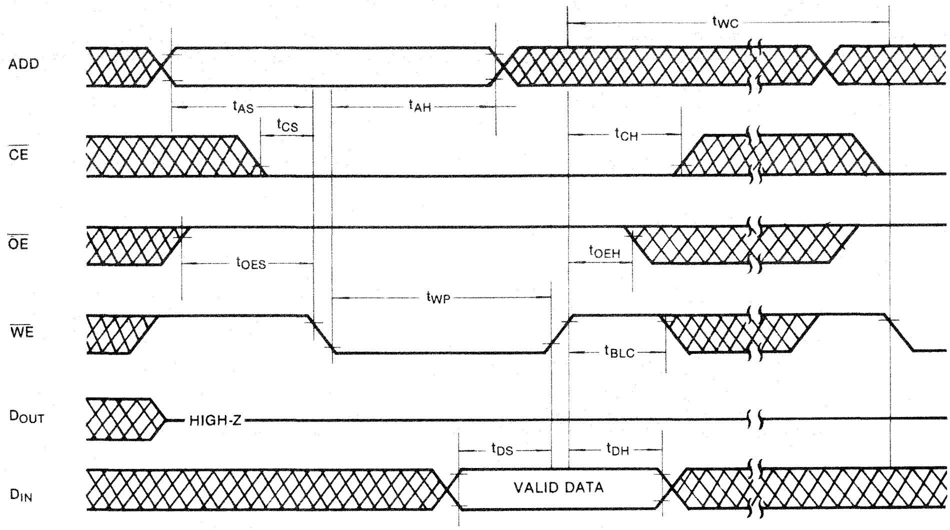
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

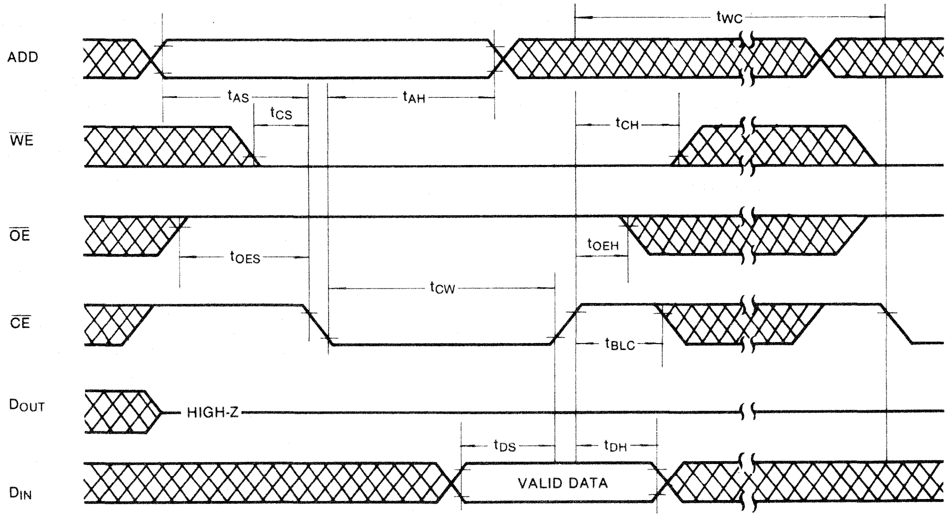


TIMING DIAGRAMS (Continued)

$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE

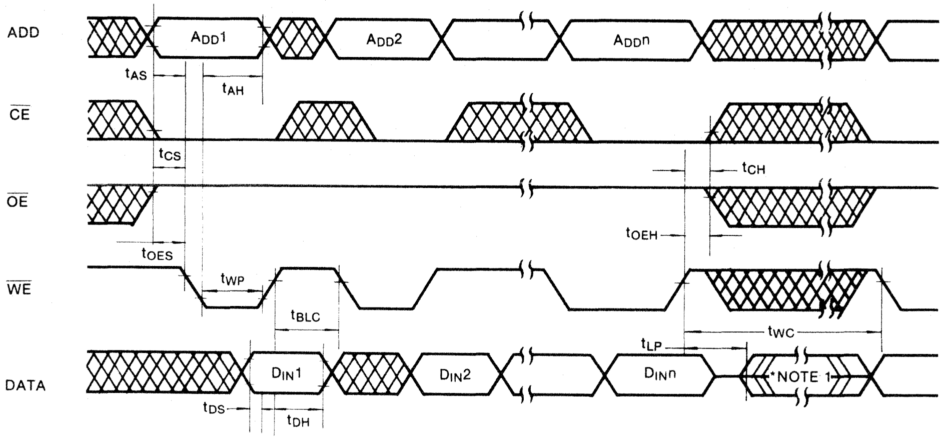


$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



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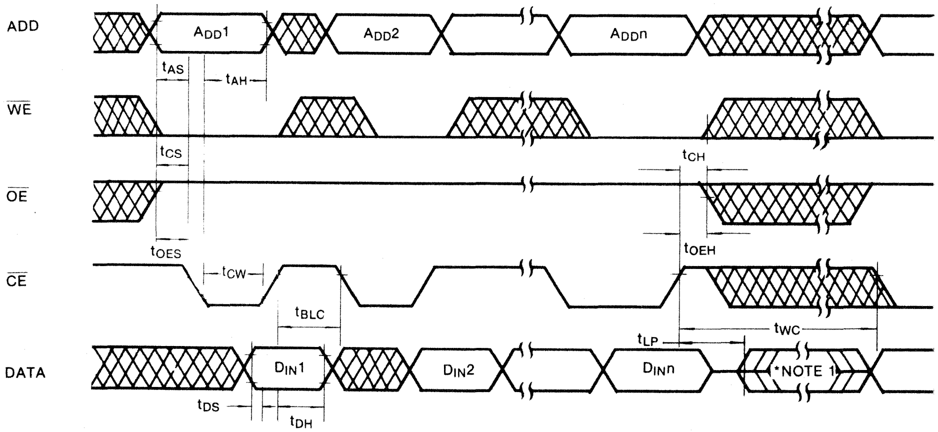

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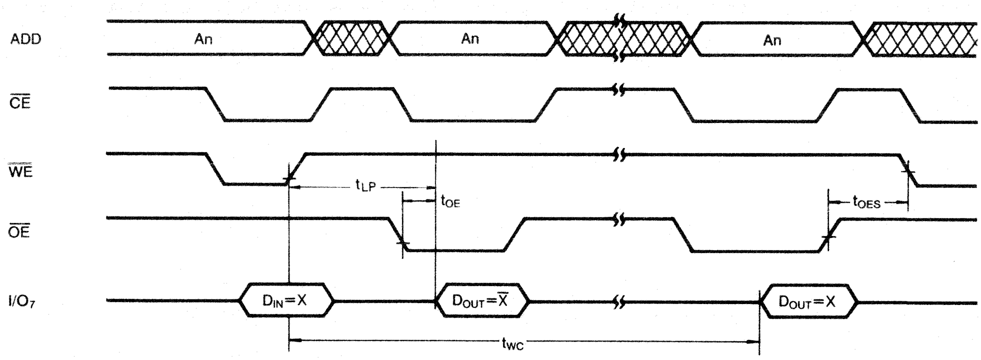
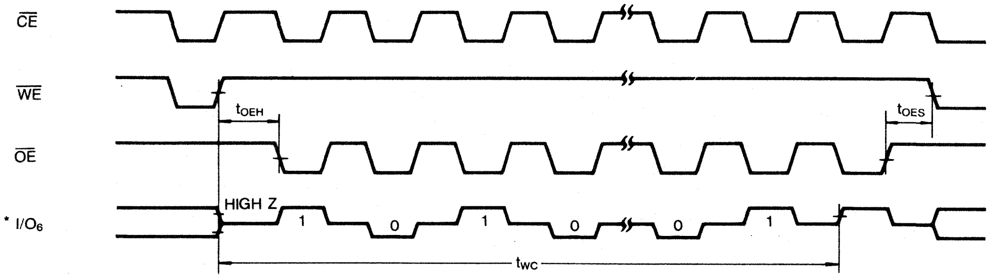
I/O_6 is toggling between "1" and "0" when the chip is successively read

TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM28C256A is similar to reading data from a SRAM. A read cycle occurs when $\overline{\text{WE}}$ is high and $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low. If either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{\text{OE}}$ or $\overline{\text{CE}}$ is high.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{\text{CE}}$. Whenever $\overline{\text{CE}}$ is high, the device is in the standby mode and I/O$_0$-I/O$_7$ are in the high impedance state, regardless of the state of $\overline{\text{OE}}$ or $\overline{\text{WE}}$.

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Writing data into the KM28C256 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

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Data is loaded into the KM28C256A by sequentially pulsing $\overline{\text{WE}}$ with $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{\text{WE}}$ and data is latched on the rising edge of $\overline{\text{WE}}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

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DEVICE OPERATION (Continued)

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**** TOGGLE BIT ****

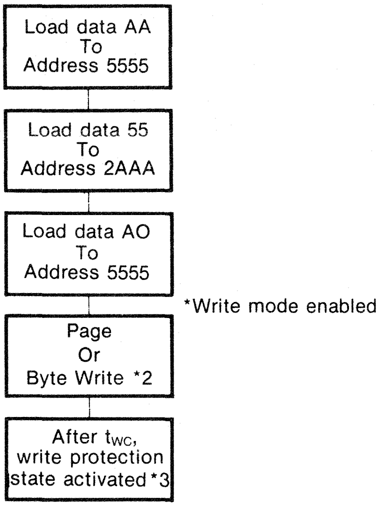
The KM28C256A also provides a toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, successive attempts to read the EEPROM will toggle I/O_6 between '1' and '0'. Once the write cycle is complete, the toggling will stop and valid data will be read.

ENDURANCE AND DATA RETENTION

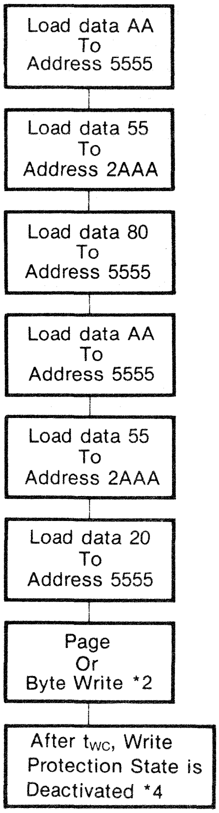
The KM28C256A is designed for applications requiring up to 100,000 write cycles per byte and ten years of data retention. This means that each byte can be reliably written 100,000 times without degrading device operation. The device also features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

SOFTWARE DATA PROTECTION ALGORITHM*1

SDP Enable Sequence



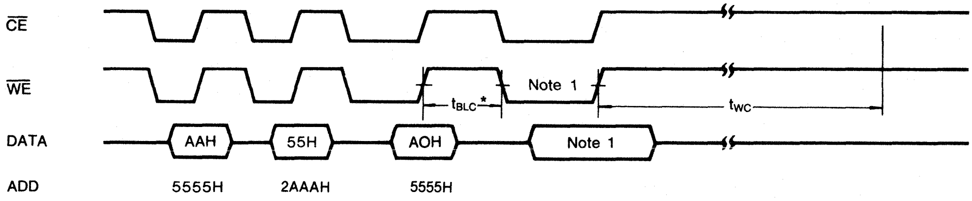
SDP Disable Sequence



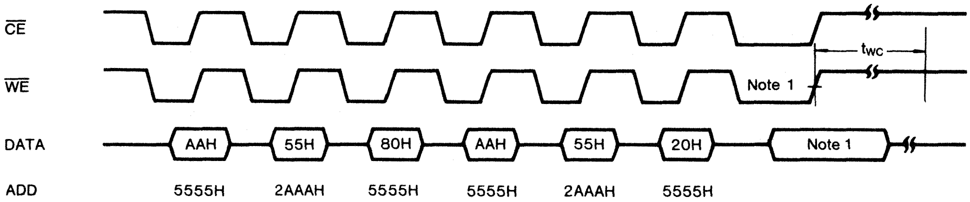
Notes 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{14}-A_0 (HEX)
2. 1 to 64-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is written.
4. Write protection state will be deactivated after t_{WC} even if no data is written.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP Enable Timing SEQUENCE



SDP Disable Timing SEQUENCE

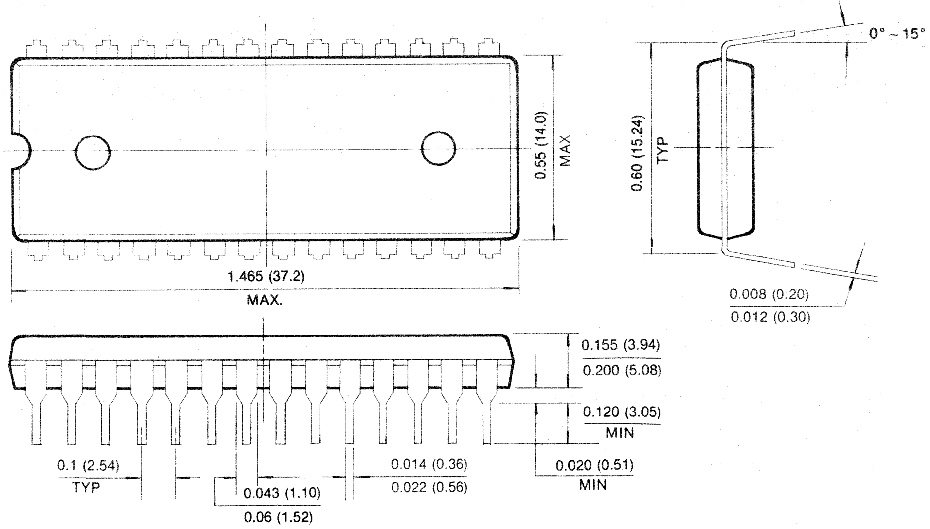


*$\leqslant t_{BLC}$ max.
Note 1 to 64 byte of data may be louded in random order.

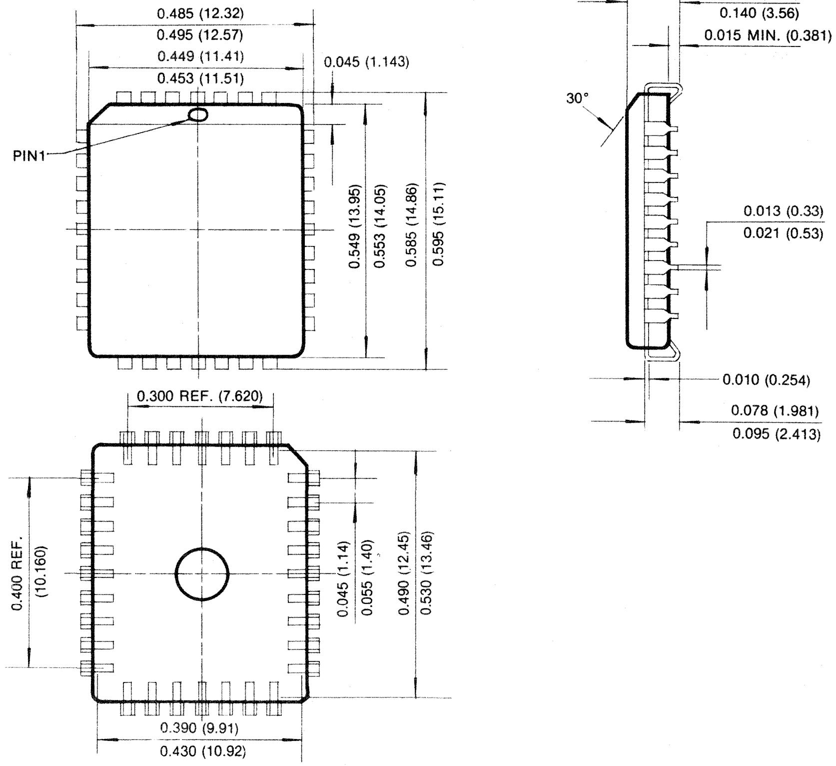
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



128K×8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Fast Read Access Time: 120ns**
- **Single 5 Voltage Supply**
- **128 Byte Page Write Operation**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Write Timing**
  - **Automatic Page Erase Before Write**
- **Fast Write Cycle Time**
  - **Page Write Time: 10ms**
  - **Chip Erase Time: 10ms**
- **Low Power Dissipation**
  - **100μA: Standby (max)**
  - **60mA: Operating (max)**
- **Hardware and Software Data Protection**
- **$\overline{\text{Data}}$ Polling and Toggle Bit**
- **Reliable CMOS Floating-Gate Technology**
  - **Endurance: 100,000**
  - **Data Retention: 10 Years**
- **JEDEC Standard Byte-wide Pinout**
  - **32-Pin DIP/PLCC/TSOP1**

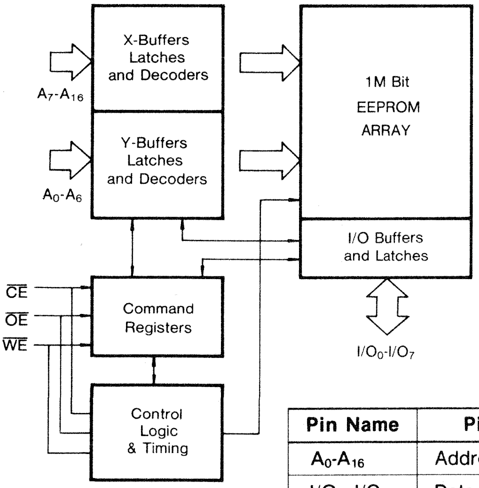
GENERAL DESCRIPTION

The KM29C010 is a 131,072×8 bit Flash-like electrically erasable programmable read only memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

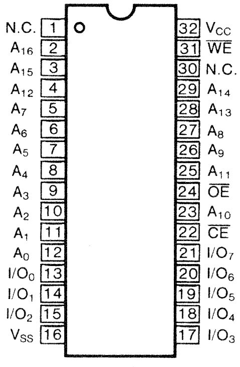
Writing data into the KM29C010 is very simple. Writing the KM29C010 is performed on a page basis; 128 bytes of data are loaded into the page buffer and then simultaneously written into the array.

The KM29C010 features $\overline{\text{Data}}$ polling and Toggle bit schemes that signal the processor an early completion of a write cycle without requiring any external hardware.

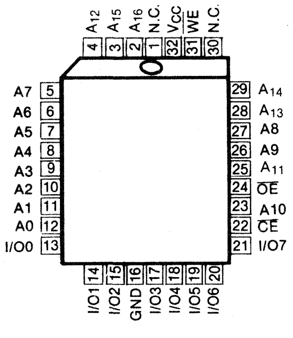
BLOCK DIAGRAM



PIN CONFIGURATION

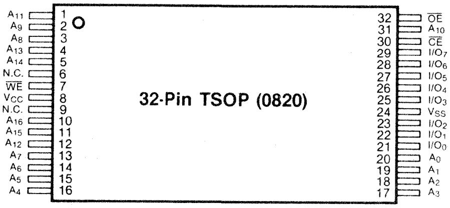


KM29C010



KM29C010J

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground



KM29C010T

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Short Circuit Output Current	I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Note: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's open (Note 1)	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3*	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 8.4MHz.
2. Programmable Write Inhibit V_{CC} Level (V_{WI}), $V_{WI} = 3.0V$ (Typ.)
3. $V_{IL}(min) = -3.0V$ for ≤10ns Pulse.

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{IO} = 0V$	—	6	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	Toggle Bit	I/O_6	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

Note: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM29C010-12		KM29C010-15		KM29C010-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Chip Enable Access Time	t_{CE}	—	120	—	150	—	200	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Output Enable Access Time	t_{OE}	—	50	—	60	—	80	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	40	0	50	0	60	ns
Output Hold from Address Change, Chip Disable	t_{OH}	0	—	0	—	0	—	ns

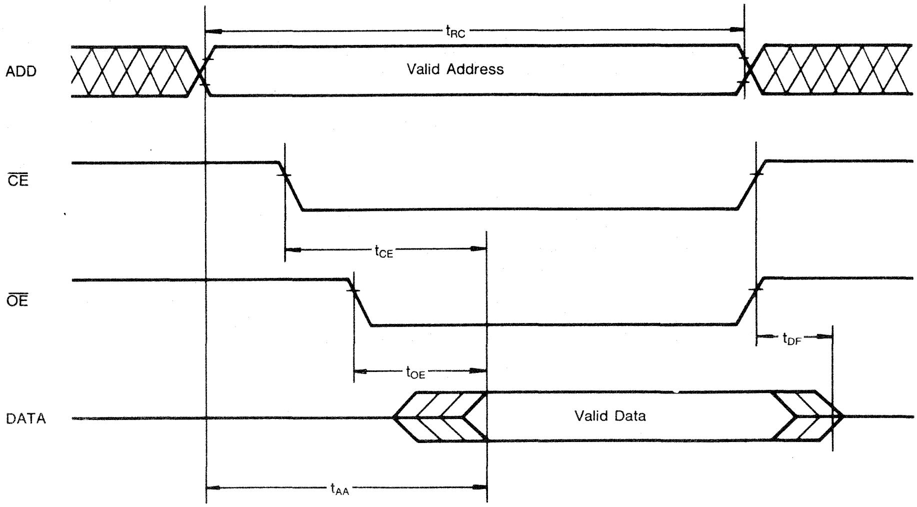
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	10	—	ms
Address Set-Up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	80	—	ns
Write Set-Up Time	t_{CS}	0	—	ns
Write Hold Time	t_{CH}	0	—	ns
$\overline{CE}$ Pulse Width	t_{CW}	100	—	ns
Output Enable Set-Up Time	t_{OES}	10	—	ns
Output Enable Hold Time	t_{OEH}	10	—	ns
$\overline{WE}$ Pulse Width	t_{WP}	100	—	ns
Data Set-Up Time	t_{DS}	50	—	ns
Data Hold Time	t_{DH}	0	—	ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to Data Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a raising edge of $\overline{WE}$.

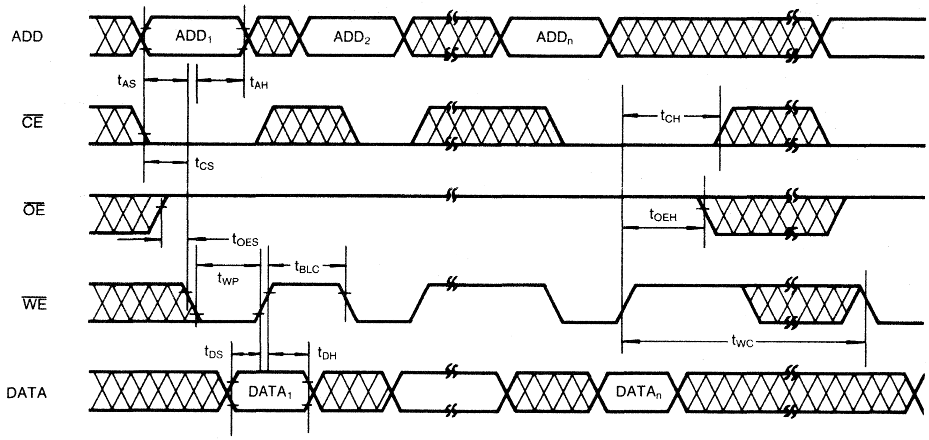
TIMING DIAGRAMS

READ CYCLE ($\overline{WE}=V_{IH}$)

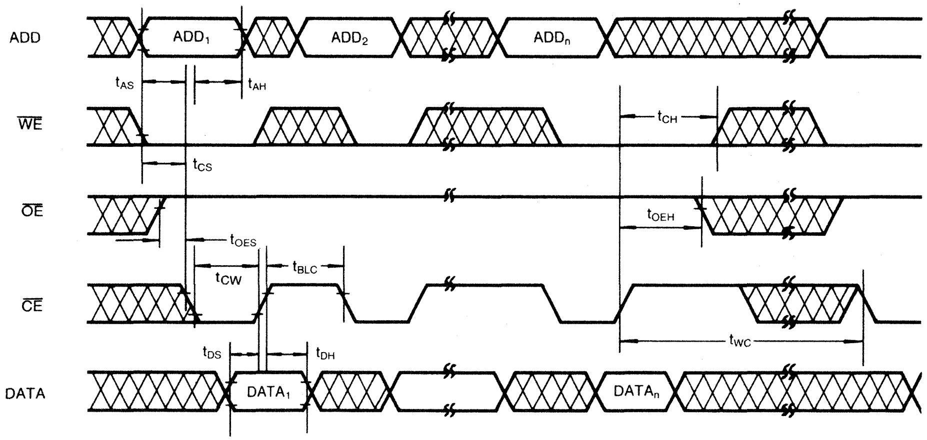


TIMING DIAGRAM (Continued)

PAGE PROGRAM CYCLE (WE Controlled Write Cycle)

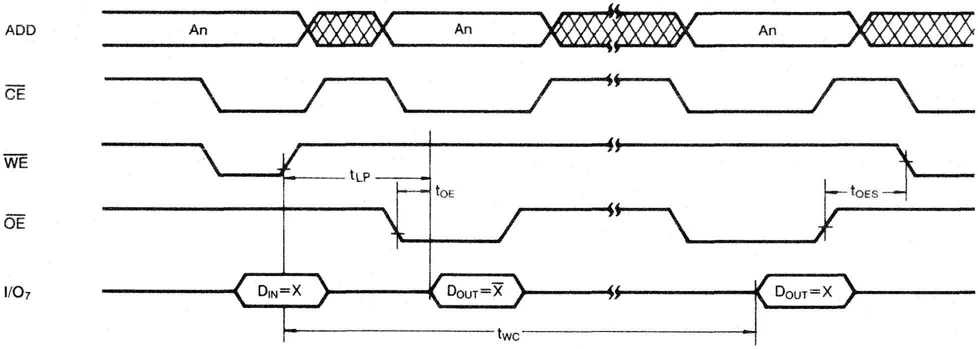


PAGE PROGRAM CYCLE (CE Controlled Write Cycle)

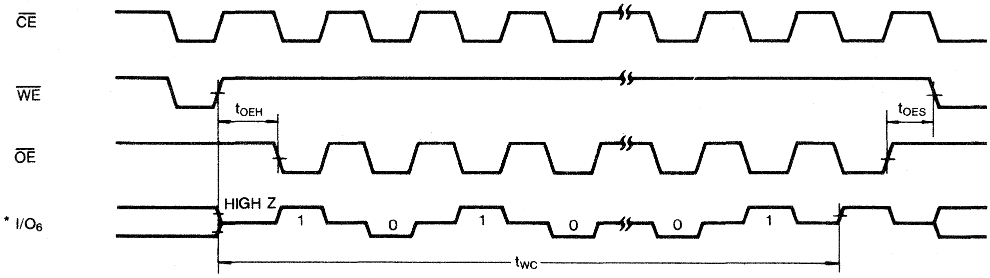


TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM29C010 is similar to reading data from a SRAM. Read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high a read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Current consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_0 \sim I/O_7$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA LOADING

A byte load is performed by appling a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_6) order and can be renewed in a data loading period.

PAGE WRITE

The KM29C010 is renewed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the write of its page will be erased to read data FFh. Once the bytes of a page are loaded into the device, they are simultaneously written during the internal write period. After the first byte data have been loaded into the device, successive bytes are entered in the same manner.

The nonvolatile write starts if $\overline{WE}$ stay high for the least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address ($A_7 \sim A_{16}$) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed during the loading period are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page.

The KM29C010 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM29C010 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM29C010 has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than V_{WI}, the write inhibit V_{CC} level. During power-up, the KM29C010 automatically prevents any write operation for a period of 5ms (max.) after V_{CC} reaches the V_{WI} level. This will protect the chip from a false write during power up transiention. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit from inadvertent writings.

** SOFTWARE DATA PROTECTION **

The KM29C010 has the JEDEC standard software data protection scheme for enhanced protection of stored data.

The shceme does not affect normal write operation if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing short SDP enable software alogrithm, followed by a page write operation. Once the protection mode is enabled, the KM29C010 will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by excuting a SDP disable software algorithm. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

$\overline{\text{DATA}}$ POLLING

The KM29C010 features $\overline{\text{DATA}}$-polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read the EEPROM will produce, at I/O_7, an inverted data of the last data loaded into the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

TOGGLE BIT

The KM29C010 also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 from "1" to "0" and "0" to "1". Once the write cycle is complete, the toggling will stop and valid data will be read.

ENDURANCE AND DATA RETENTION

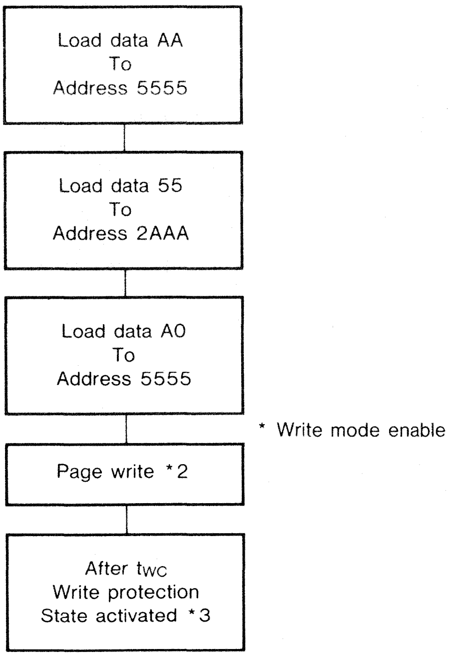
The KM29C010 is designed for applications requiring up to 100,000 write cycles per page and ten years of data retention. This means that each bit can be reliably written 100,000 times without degrading device opera-

DEVICE OPERATION (Continued)

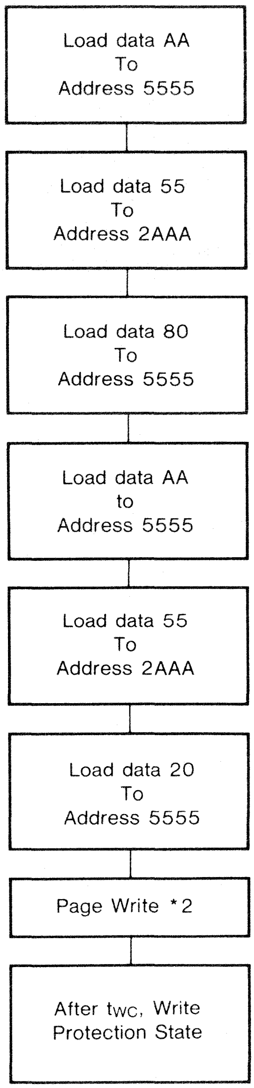
tion, and this device features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in 32 bits. And hence, significant improvements in the endurance and data retention characteristics are achieved.

SOFTWARE DATA PROTECTION ALGORITHM *1

SDP Enable Sequence



SDP Disable Sequence



Note 1. Data format: I/O$_7$~I/O$_0$ (HEX)
Address format: A_{16}~A_0 (HEX)
2. 1 to 128-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC}.
4. Write protection state will be deactivated after t_{WC}.

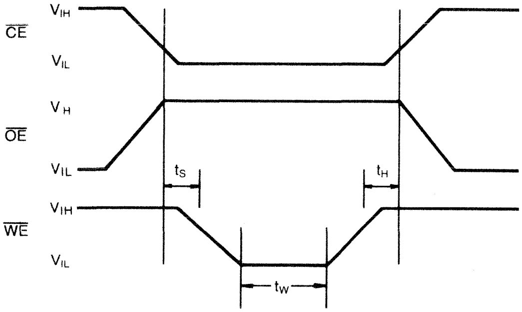
SOFTWARE CHIP ERASE

The KM29C010 may be erased at one time by using a six byte software command code. The erase code consists of six byte load commands to specify address location and data patterns. Once the code has been entered the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will automatically start the erase operation so that external clocks are not required.

HIGH VOLTAGE CHIP ERASE

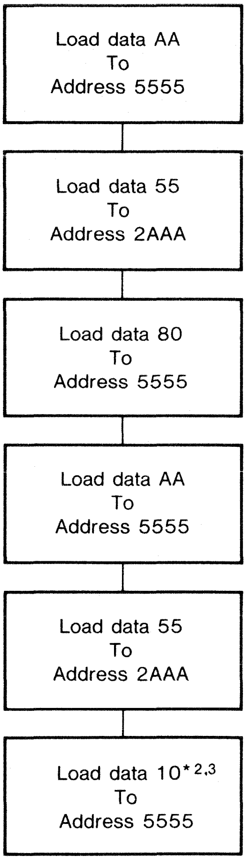
The contents of the KM29C010 may be set to the high state (FFh) by using an externally controlled high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high: When $\overline{WE}$ pulsed low for a minimum of 10ms, the contents of the KM29C010 is erased.

HIGH VOLTAGE CHIP ERASE WAVEFORMS



$t_S = t_H = 5\mu sec$ (min)
$t_W = 10msec$ (min)
$V_H = 12.0V$

SOFTWARE CHIP ERASE ALGORITHM *1



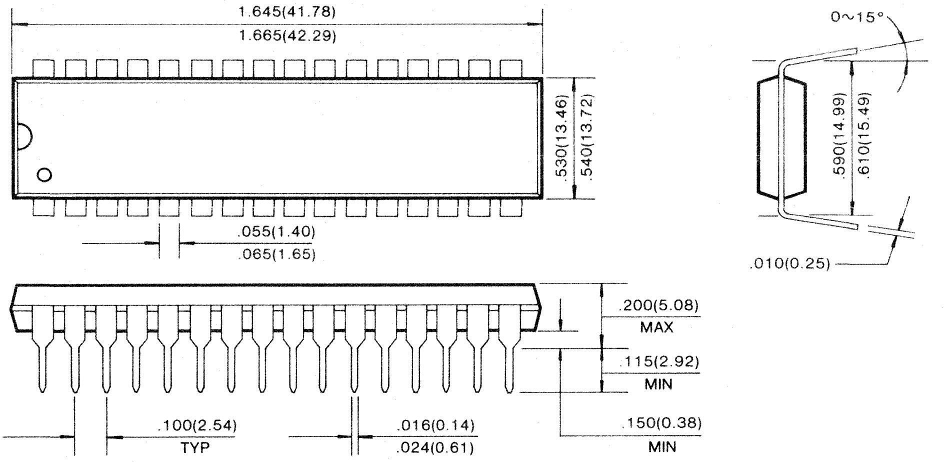
Notes for software ship erase code;

1. Data format: $I/O_7 \sim I/O_0$ (Hex.)
   Address format: $A_{16} \sim A_0$ (Hex.)
2. Data polling may be used to determine the end of the erase cycle by checking any address for data equal to FFh.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

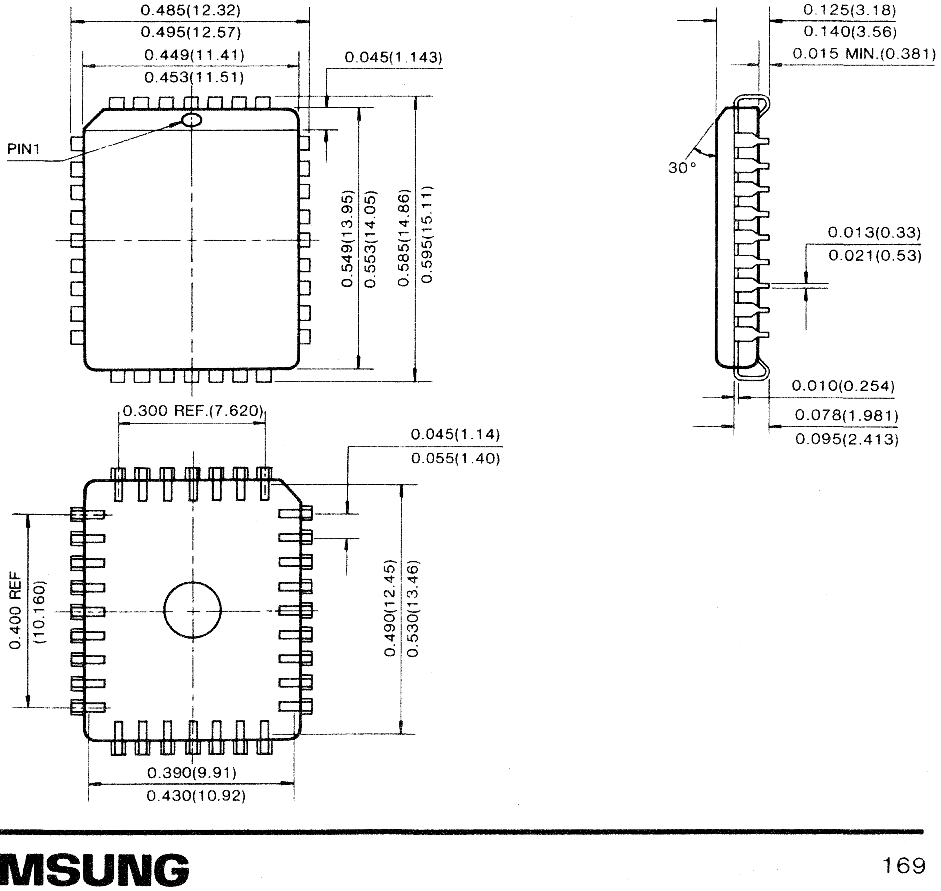
PACKAGE DIEMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)

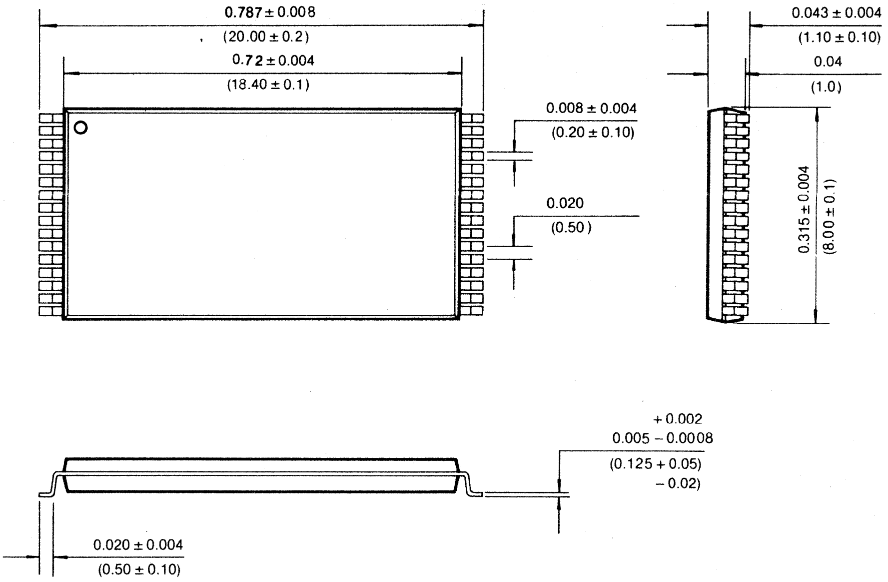


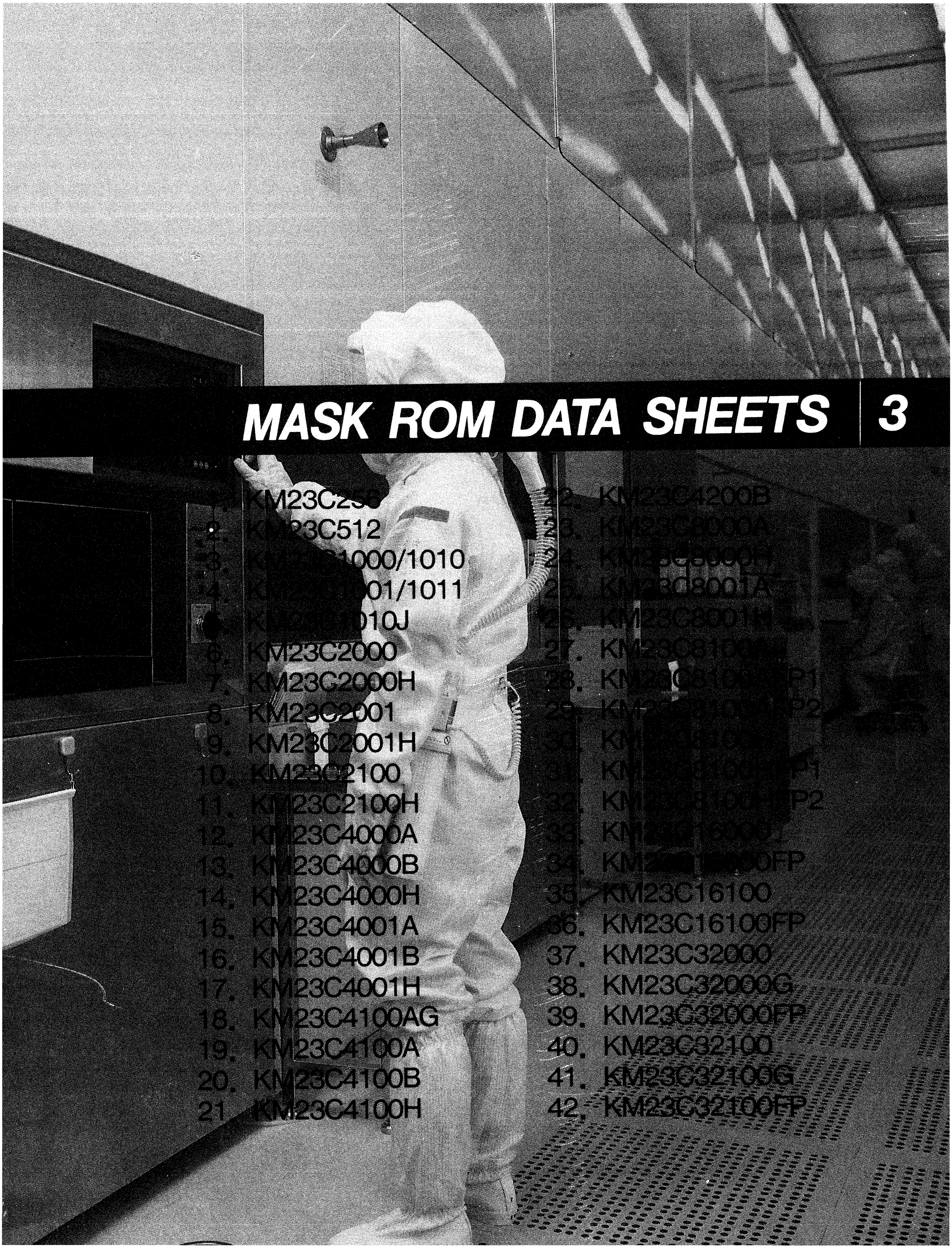
32 PIN PLASTIC LEADED CHIP CARRIER



32 PIN THIN SMALL OUTINE PACKAGE (Forward Type)

Unit: Inches (millimeters)





MASK ROM DATA SHEETS

3

1. KM23C256
2. KM23C512
3. KM23C1000/1010
4. KM23C1001/1011
5. KM23C1010J
6. KM23C2000
7. KM23C2000H
8. KM23C2001
9. KM23C2001H
10. KM23C2100
11. KM23C2100H
12. KM23C4000A
13. KM23C4000B
14. KM23C4000H
15. KM23C4001A
16. KM23C4001B
17. KM23C4001H
18. KM23C4100AG
19. KM23C4100A
20. KM23C4100B
21. KM23C4100H
22. KM23C4200B
23. KM23C8000A
24. KM23C8000H
25. KM23C8001A
26. KM23C8001H
27. KM23C8100A
28. KM23C8100AFP1
29. KM23C8100AFP2
30. KM23C8100H
31. KM23C8100HFP1
32. KM23C8100HFP2
33. KM23C16000
34. KM23C16000FP
35. KM23C16100
36. KM23C16100FP
37. KM23C32000
38. KM23C32000G
39. KM23C32000FP
40. KM23C32100
41. KM23C32100G
42. KM23C32100FP

256K-Bit (32K×8) CMOS MASK ROM

FEATURES

- **KM23C256: 28-pin DIP (Polarity programmable chip enable pin and output enable pin)**
- **KM23C256G: 32-pin SOP (Polarity programmable chip enable pin and output enable pin)**
- **32,768 × 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

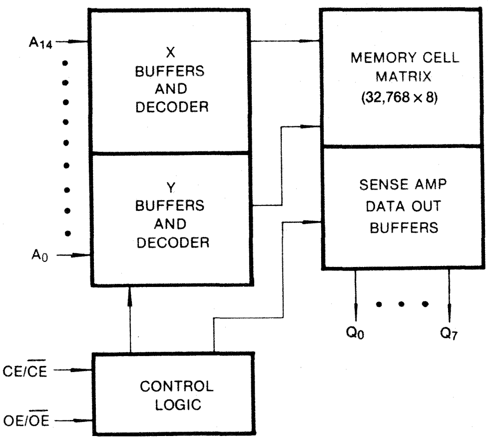
The KM23C256 is a fully static mask programmable ROM organized 32,768×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

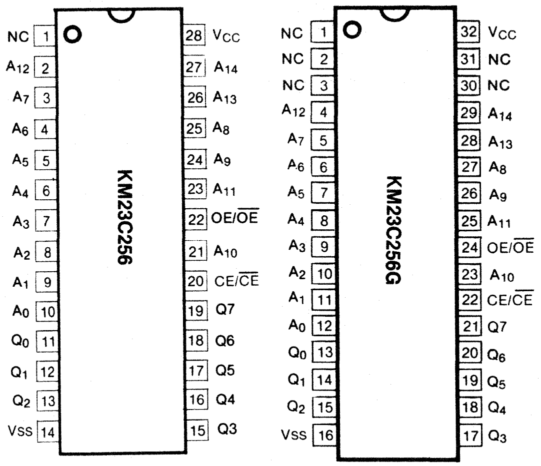
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C256 is packaged in a 28-DIP, provides polarity programmable CE and OE buffer as user option mode, the KM23C256G in a 32-SOP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N C	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $f = 5.0MHz$ all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, $f = 1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

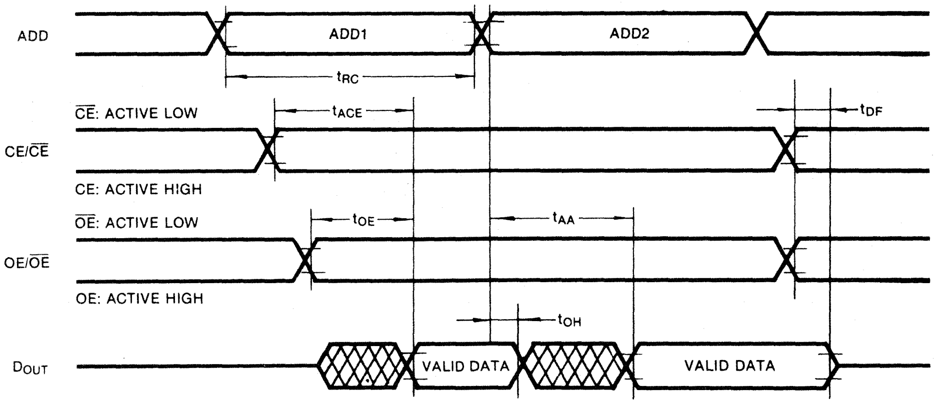
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C256(G)-12		KM23C256(G)-15		KM23C256(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

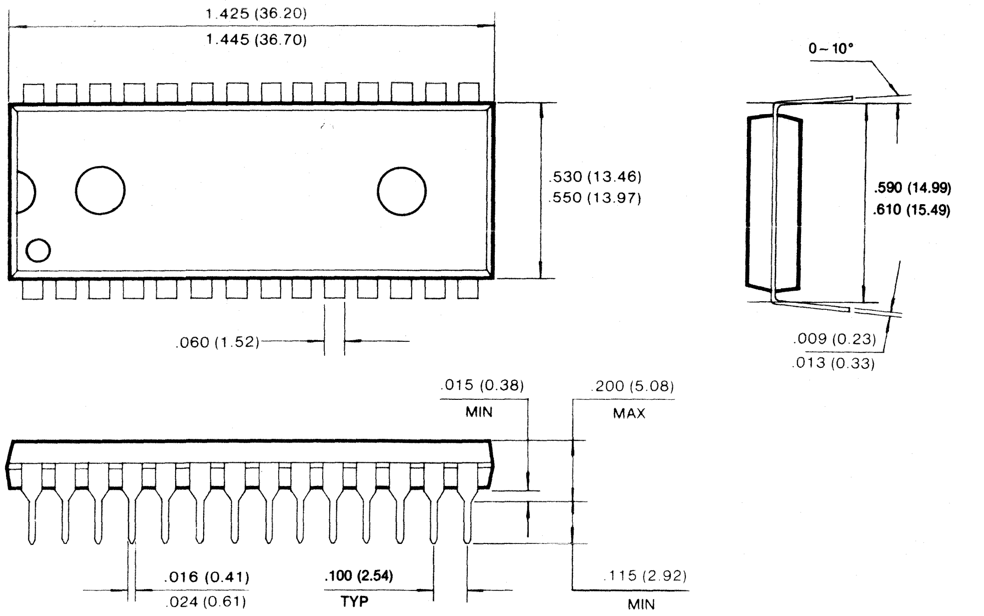
READ



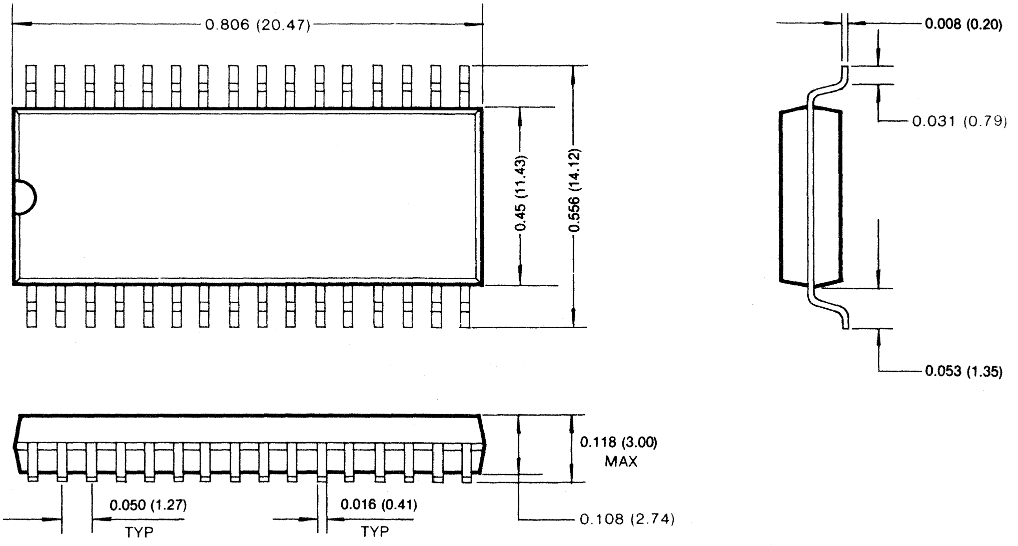
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C256)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C256G)



SAMSUNG ROM DATA INFORMATION

1. HARD MEDIA

There are many kinds of hard media to deliver ROM Code as follows, and SEC defined the priority numbers for easy access to SEC's ROM Code generation tool.

* Priority #1: Cartridge (150MB Quad Cartridge)
#2: Reel tape (6250 bpi, 9 track)
#3: EPROM (and types of EPROM)
#4: Floppy diskette (3.5 or 5.25 inch)

2. DATA FORMAT

In the event of providing ROM Code by cartridge, reel tape, or floppy diskette, SEC likes data format to be provide according to following priority.

* Priority #1: Extended Tek. Hexa format
#2: Intel-86 format
#3: Intel-8 format

3. ROM CODE TRANSPORTATION VIA SATELLITE

SEC offers ROM Code transmission through satellite and it is very much competitive way in terms of TAT compare to ROM Code exchange by mail just like DHL or SPEED POST.

512K-Bit (64K × 8) CMOS MASK ROM

FEATURES

- **KM23C512: 28-pin DIP**
  (Polarity programmable chip enable pin and output enable pin)
- **KM23C512G: 32-pin SOP**
  (Polarity programmable chip enable pin and output enable pin)
- **65,536 × 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

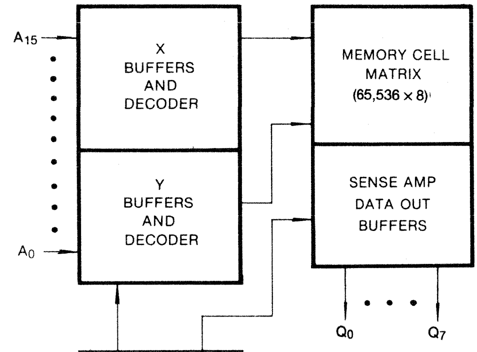
The KM23C512 is a fully static mask programmable ROM organized 65,536 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

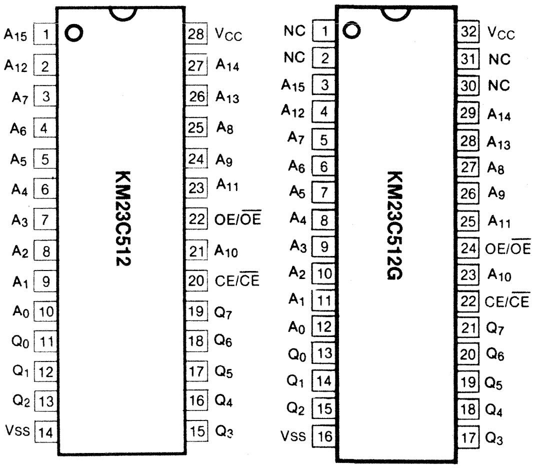
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C512 is packaged in a 28-DIP, provides polarity programmable CE and OE buffer as user option mode, the KM23C512G in a 32-SOP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

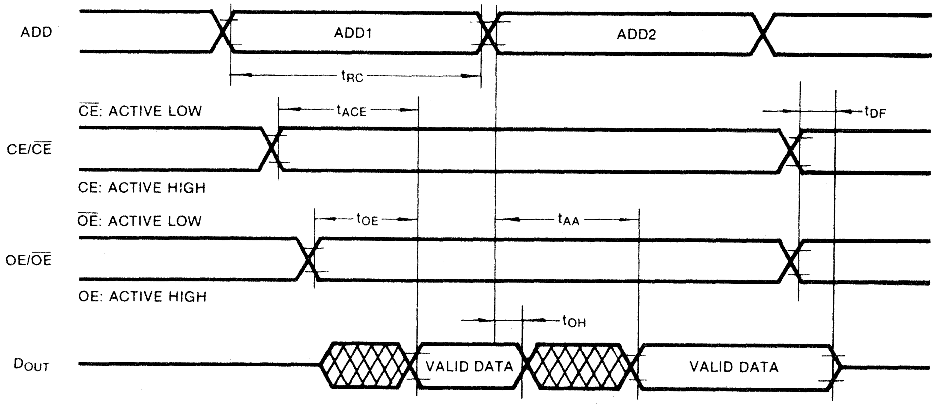
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C512(G)-12		KM23C512(G)-15		KM23C512(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

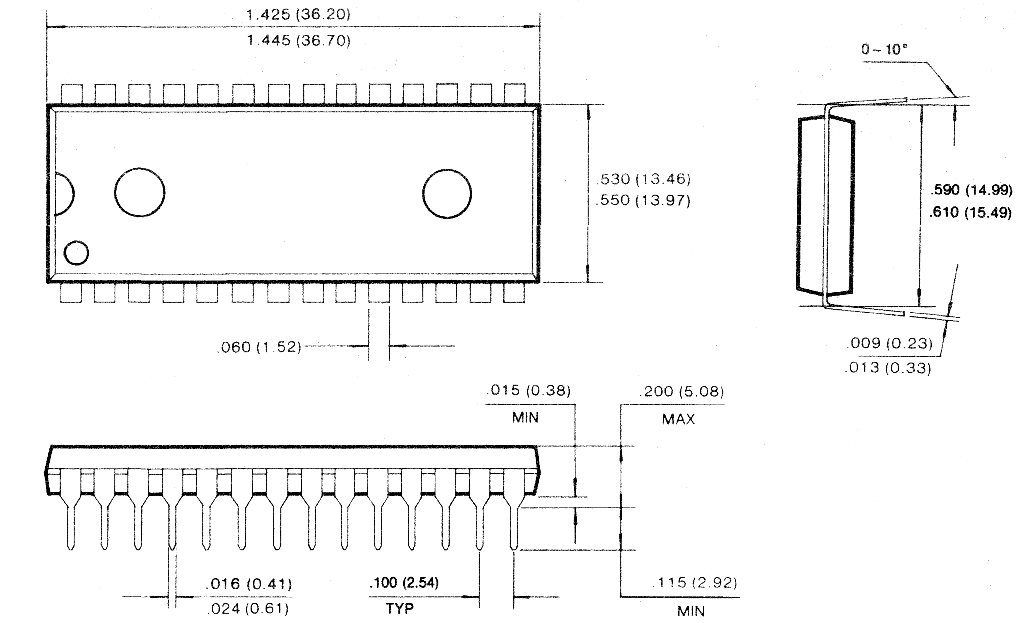
READ



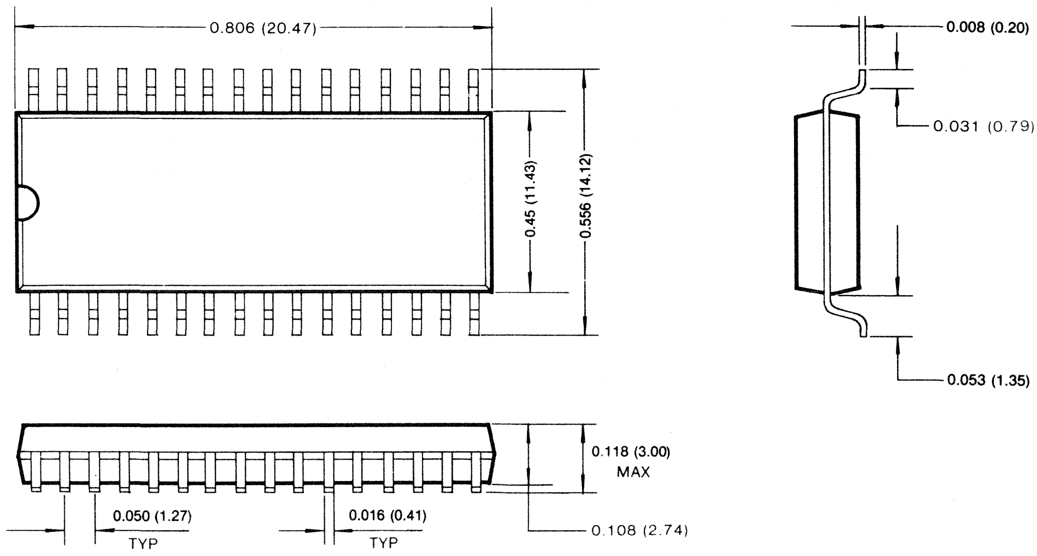
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C512)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C512G)



1M-Bit (128K×8) CMOS MASK ROM

FEATURES

- **KM23C1000: 28-pin DIP (Polarity programmable chip enable pin)**
- **KM23C1010: 32-pin DIP (Polarity programmable chip enable pin and output enable pin)**
- **131,072×8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

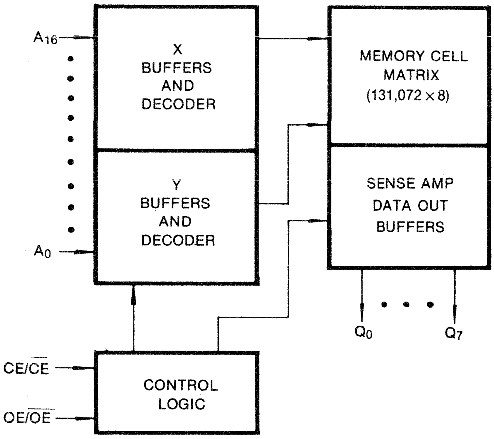
The KM23C1000/1010 is a fully static mask programmable ROM organized 131,072×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

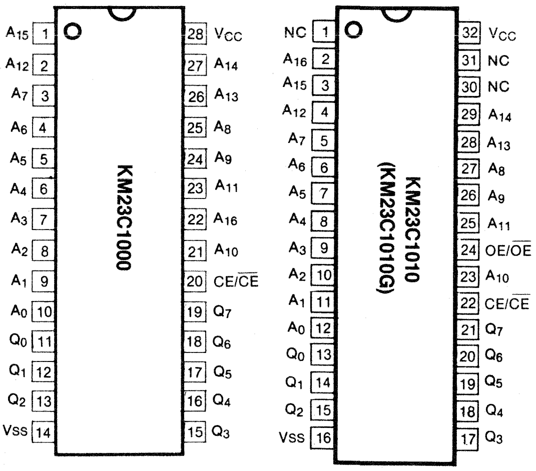
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C1000 is packaged in a 28-DIP, provides polarity programmable CE buffer as user option mode, the KM23C1010 in a 32-DIP, and the KM23C1010G in a 32-SOP, polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION (KM23C1000)

CE/$\overline{CE}$	Mode	Data	Power
L/H	Standby	High-Z	Standby
H/L	Operating	D_{OUT}	Active

MODE SELECTION (KM23C1010)

CE/$\overline{\text{CE}}$	OE/$\overline{\text{OE}}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

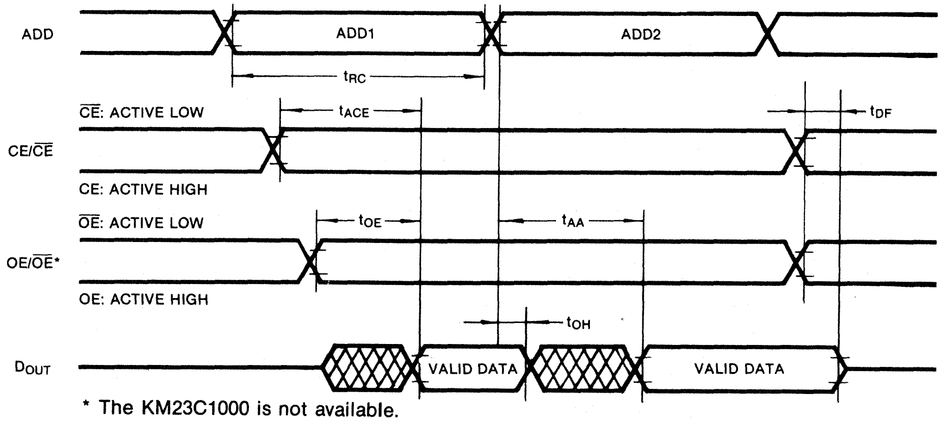
item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C1000-12 KM23C1010(G)-12		KM23C1000-15 KM23C1010(G)-15		KM23C1000-20 KM23C1010(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

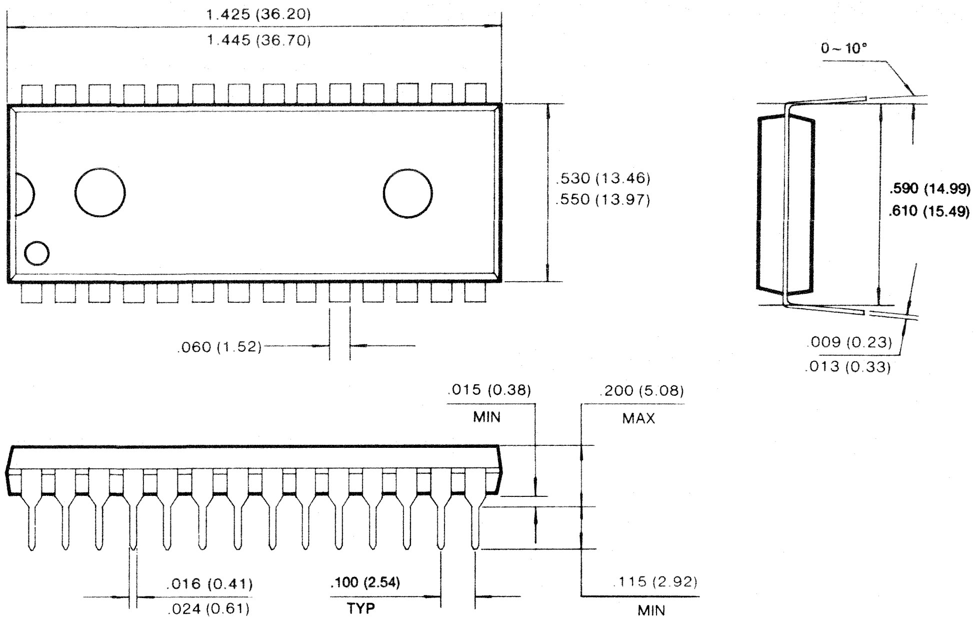


* The KM23C1000 is not available.

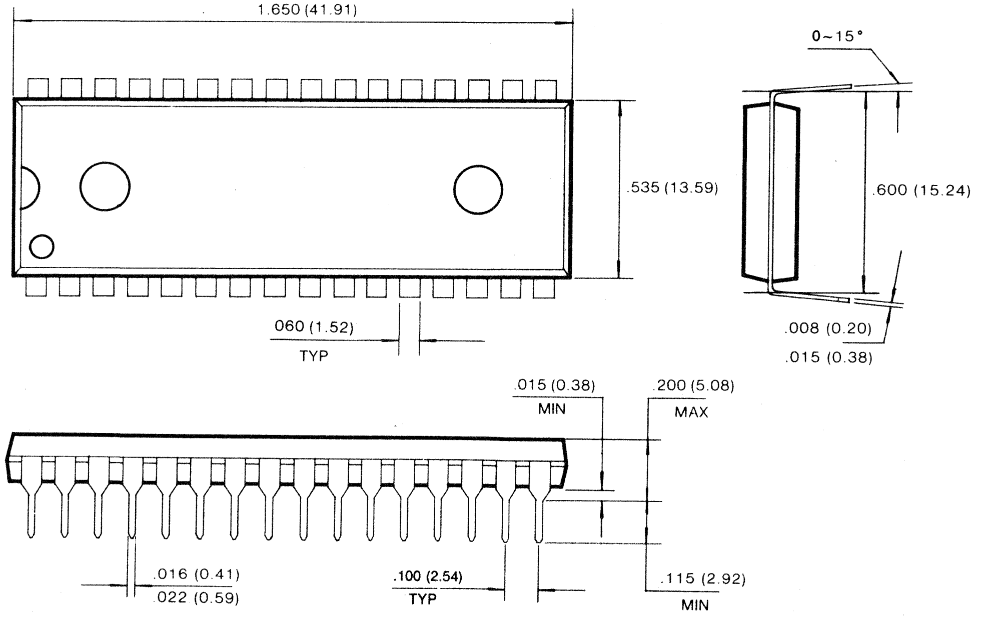
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1000)

Units: Inches (millimeters)



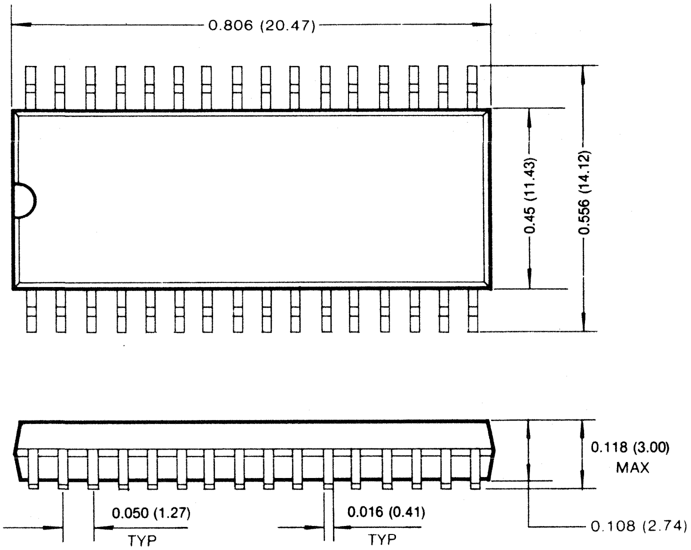
32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1010)

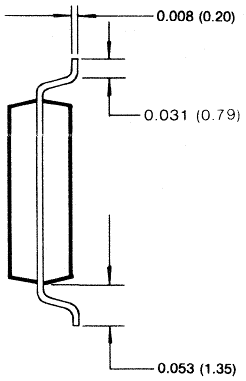


PACKAGE DIMENSIONS (Continued)

32 LEAD SMALL OUTLINE PACKAGE (KM23C1010G)

Units: Inches (millimeters)





1M-Bit (128K × 8) CMOS MASK ROM

FEATURES

- **KM23C1001: 28-pin DIP**
  (Polarity programmable output enable pin)
- **KM23C1011: 32-pin DIP**
  (Polarity programmable output enable pin)
- **131,072 × 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 40mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

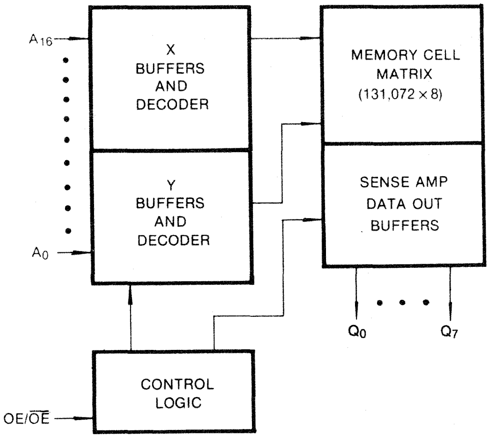
The KM23C1001/1011 is a fully static mask programmable ROM organized 131,072 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

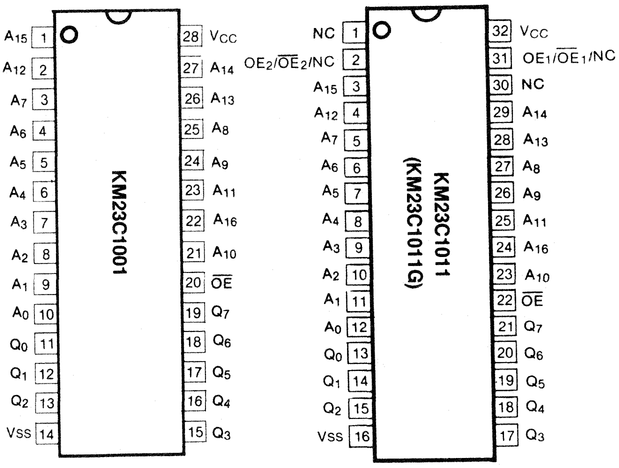
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C1001 is packaged in a 28-DIP, provides polarity programmable OE buffer as user option mode, the KM23C1011 in a 32-DIP, and the KM23C1011G in a 32-SOP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, $f = 5.0$MHz all output open	—	40	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$mA	—	0.4	V

CAPACITANCE ($T_A = 25$°C, $f = 1.0$MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

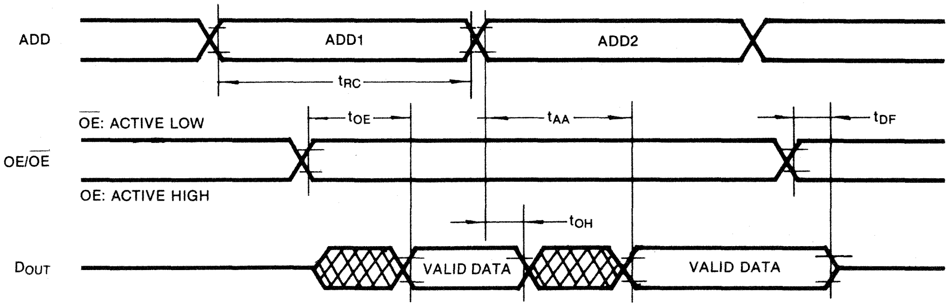
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C1001-12 KM23C1011(G)-12		KM23C1001-15 KM23C1011(G)-15		KM23C1001-20 KM23C1011(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

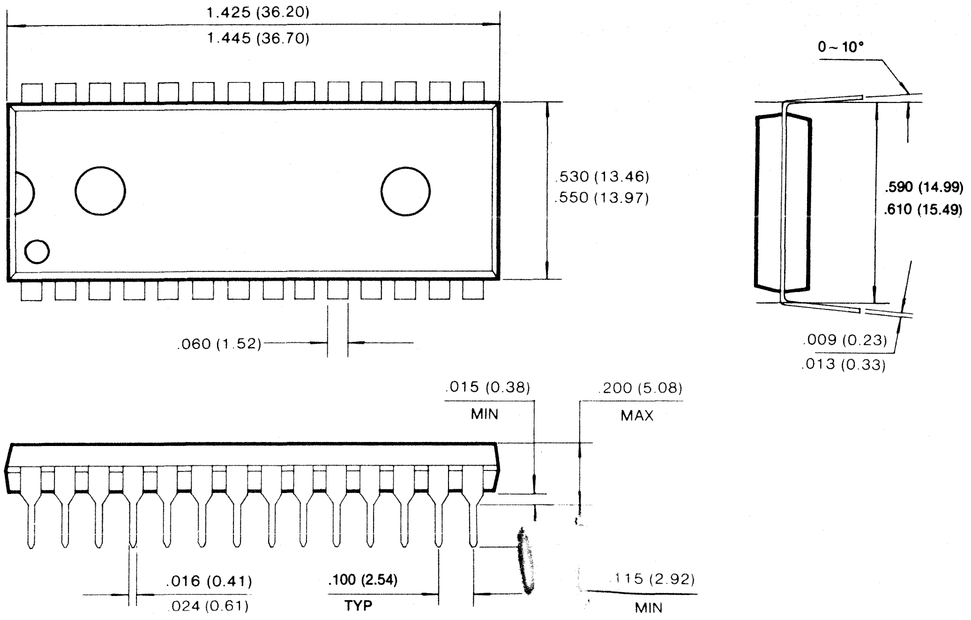
READ



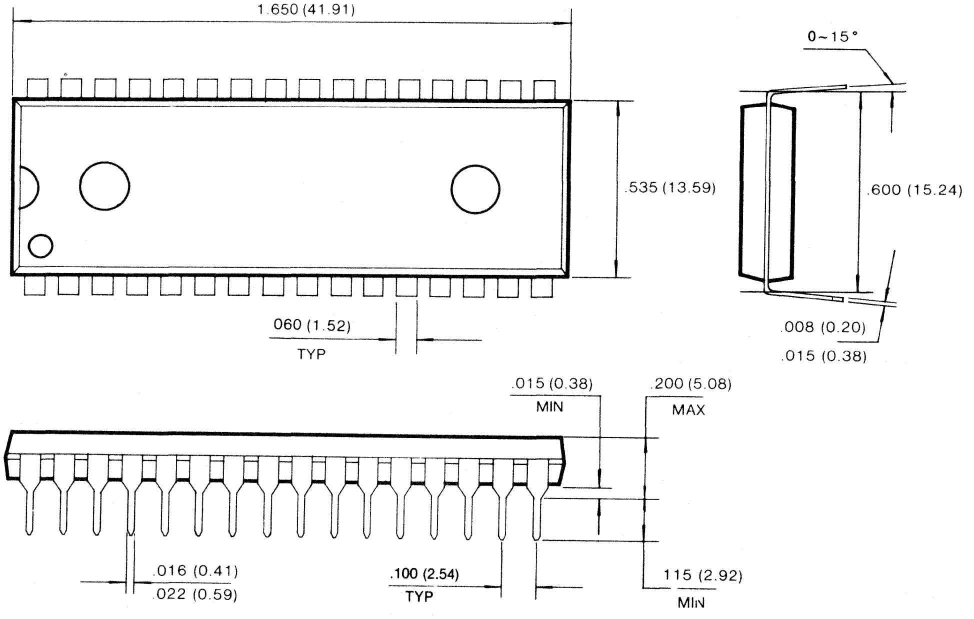
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1001)

Units: Inches (millimeters)



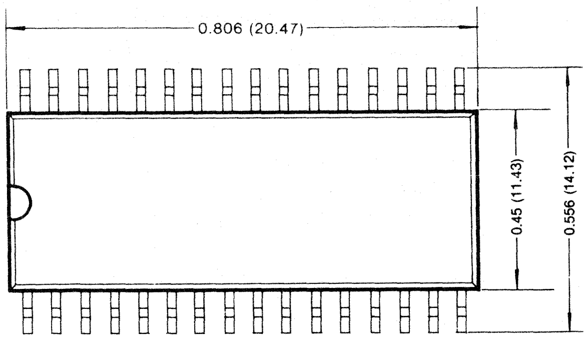
32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1011)

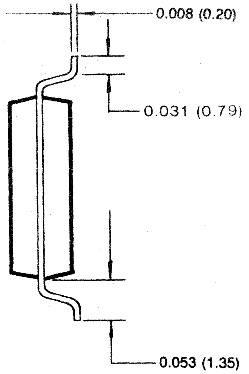


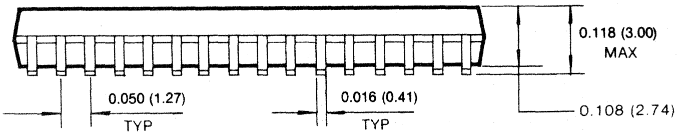
PACKAGE DIMENSIONS (Continued)

32 LEAD SMALL OUTLINE PACKAGE (KM23C1011G)

Units: Inches (millimeters)







1M-Bit (128K×8) CMOS MASK ROM

FEATURES

- **KM23C1010J: 32-pin PLCC (Polarity programmable chip enable pin and output enable pin)**
- **131,072×8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**

GENERAL DESCRIPTION

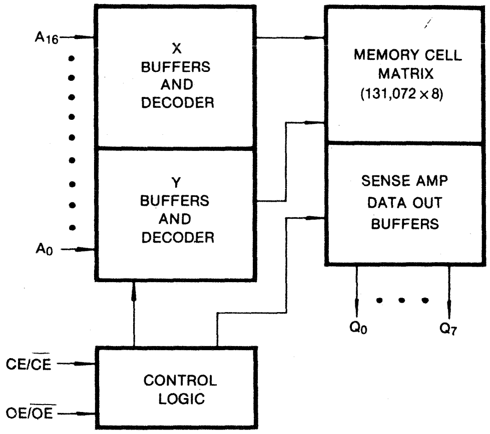
The KM23C1010J is a fully static mask programmable ROM organized 131,072×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

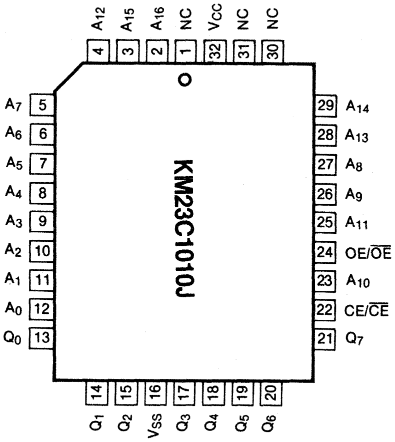
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C1010J is packaged in a 32 PLCC, polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $f = 5.0$MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$mA	—	0.4	V

CAPACITANCE ($T_A = 25$°C, $f = 1.0$MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

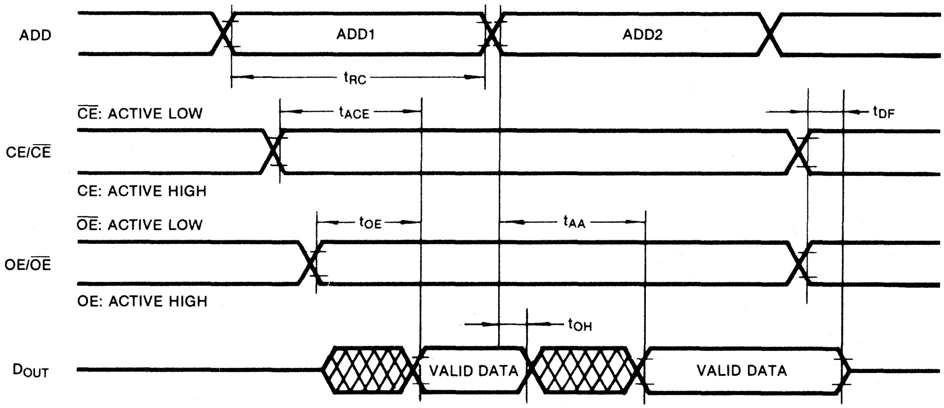
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C1010J-12		KM23C1010J-15		KM23C1010J-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

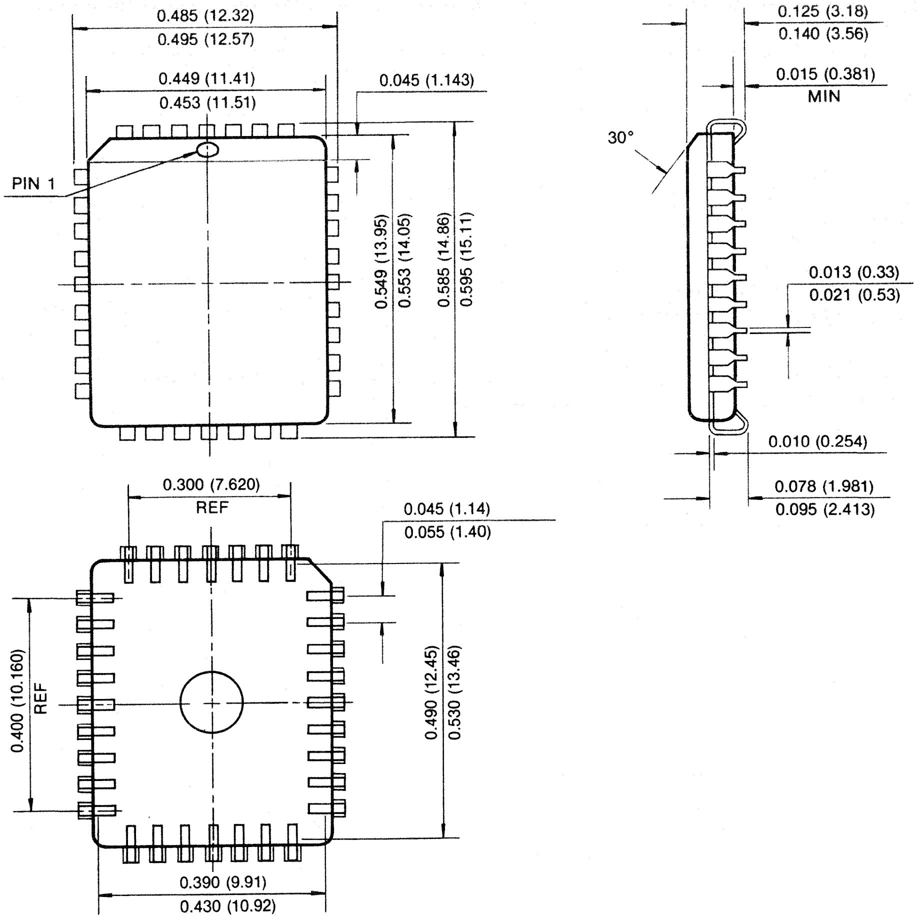
READ



PACKAGE DIMENSIONS

32 PIN PLASTIC LEADED CHIP CARRIER (KM23C1010J)

Units: Inches (millimeters)



2M-Bit (256K × 8) CMOS MASK ROM

FEATURES

- **262,144 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP (JEDEC standard)**
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

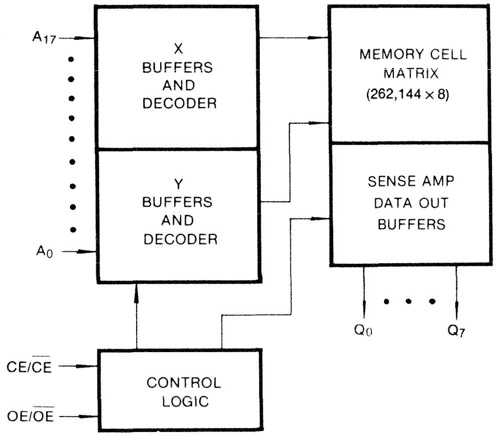
The KM23C2000 is a fully static mask programmable ROM organized 262,144 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

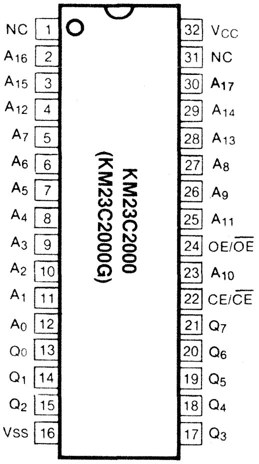
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C2000 is packaged in a 32-DIP, and the KM23C2000G in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

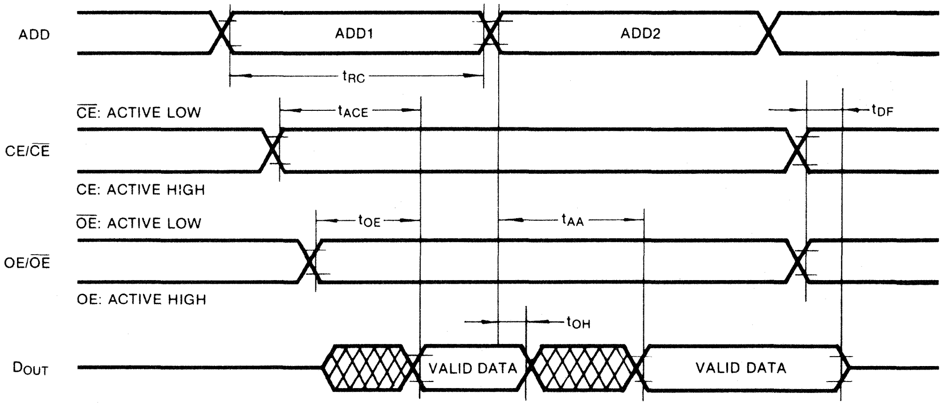
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2000(G)-15		KM23C2000(G)-20		KM23C2000(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

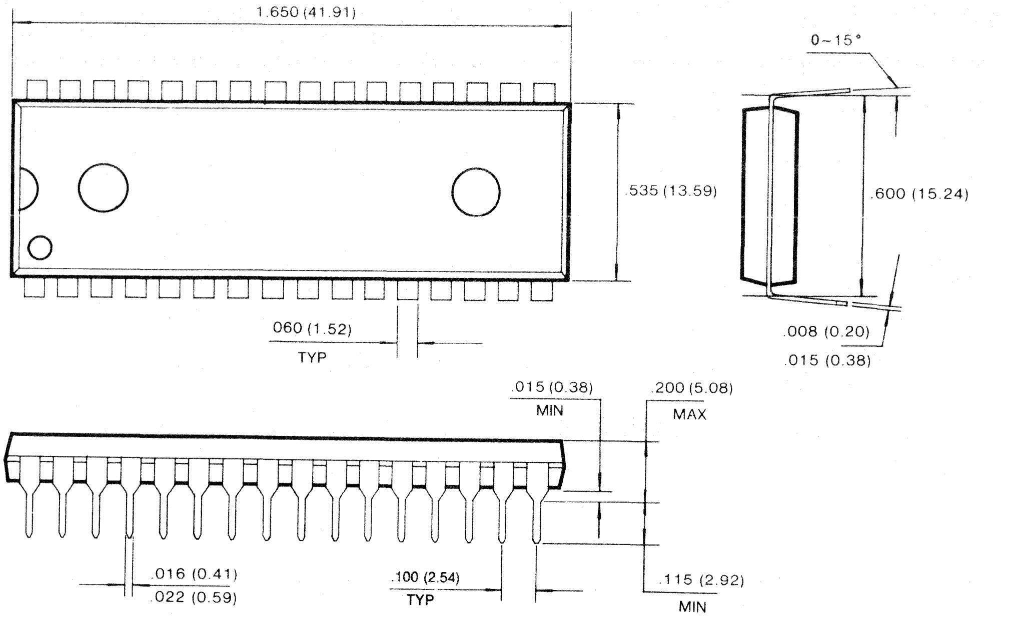
READ



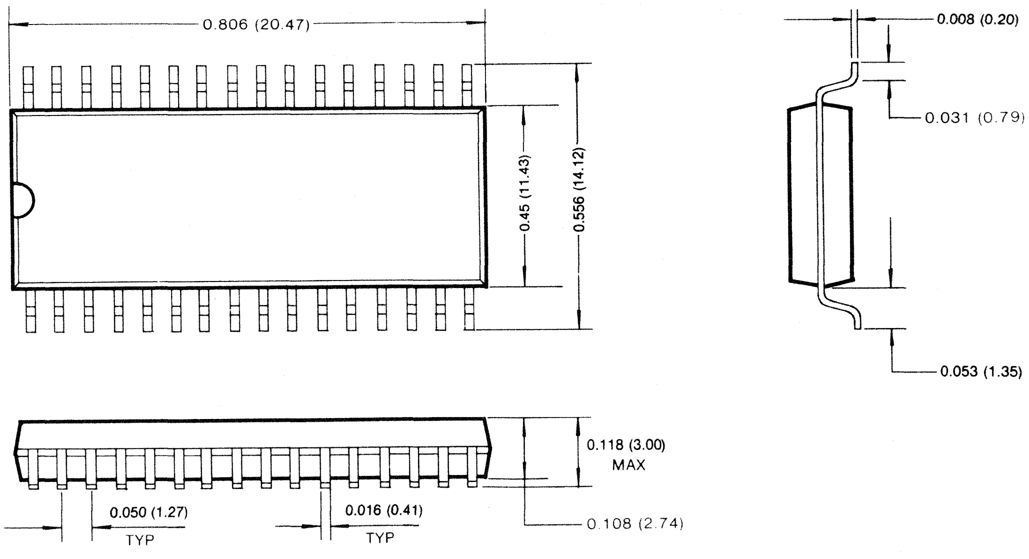
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2000)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2000G)



2M-Bit (256K × 8) CMOS MASK ROM

FEATURES

- **262,144 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 40mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

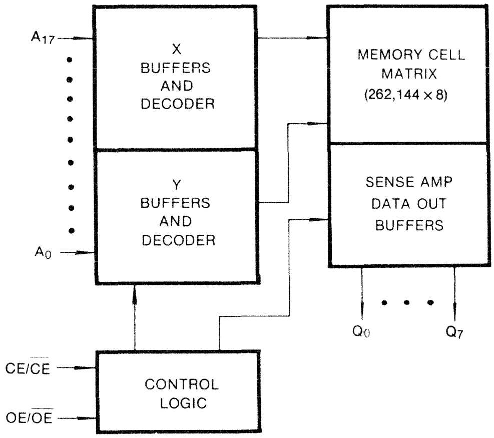
The KM23C2000H is a fully static mask programmable ROM organized 262,144 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

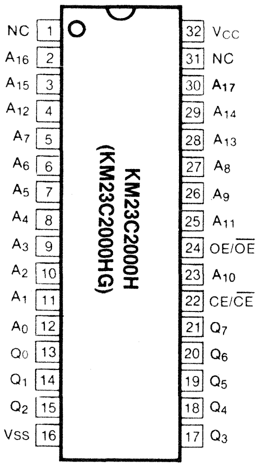
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C2000H is packaged in a 32-DIP, and the KM23C2000HG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

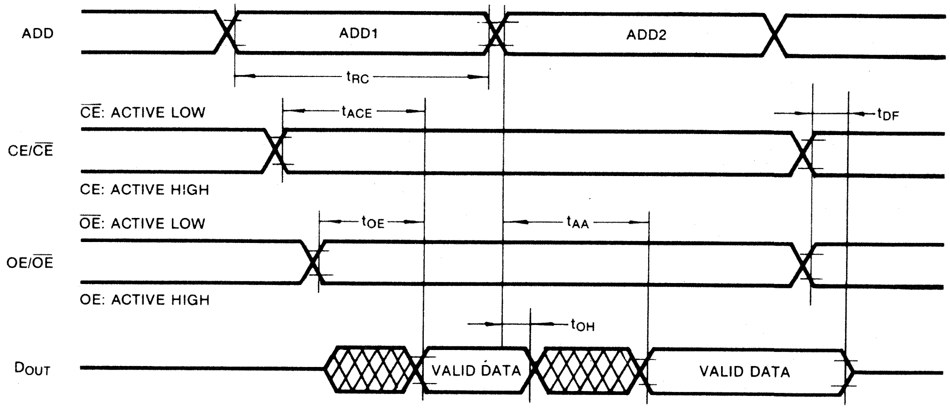
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2000H(G)-10		KM23C2000H(G)-12		KM23C2000H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

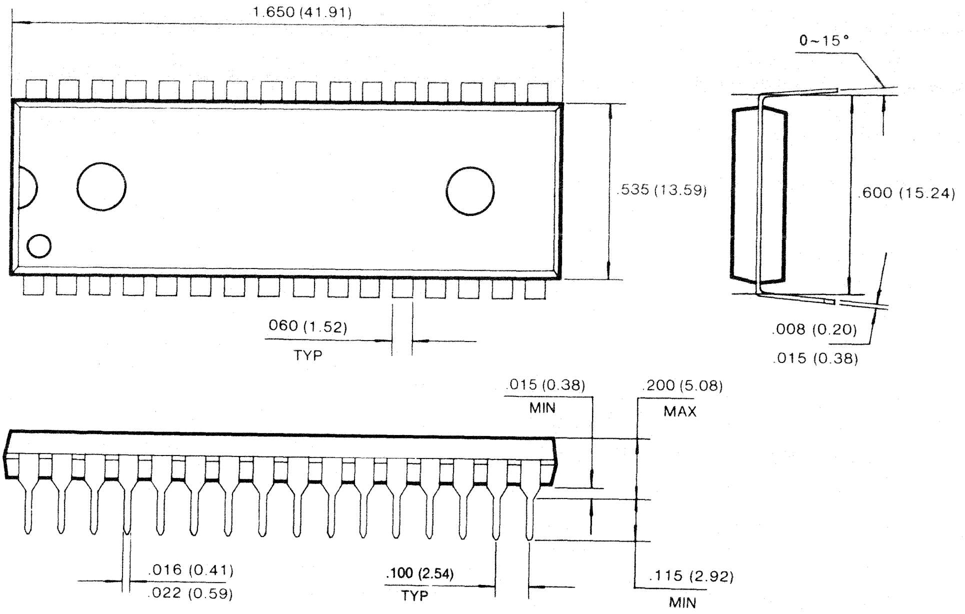
READ



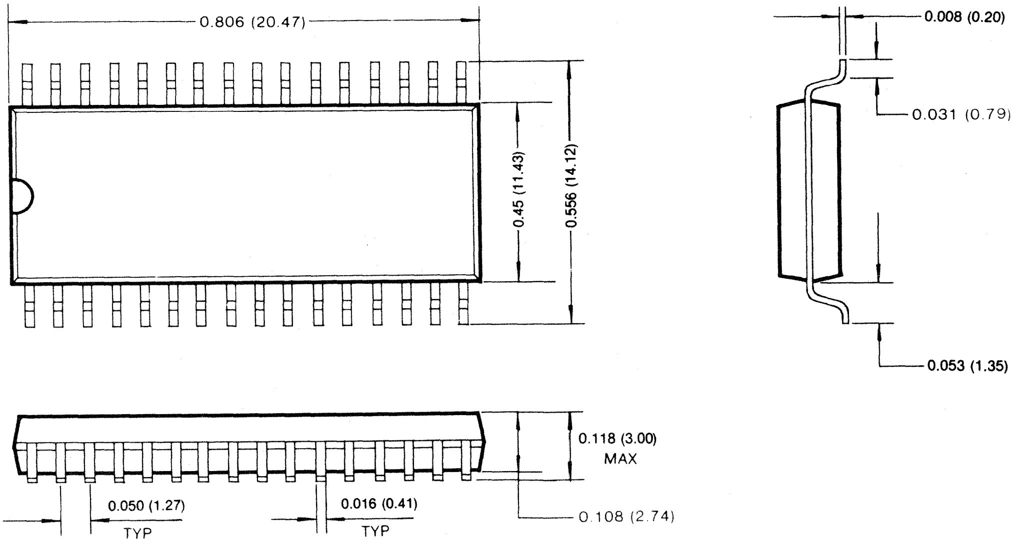
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2000H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2000HG)



2M-Bit (256K × 8) CMOS MASK ROM

FEATURES

- **262,144 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**

GENERAL DESCRIPTION

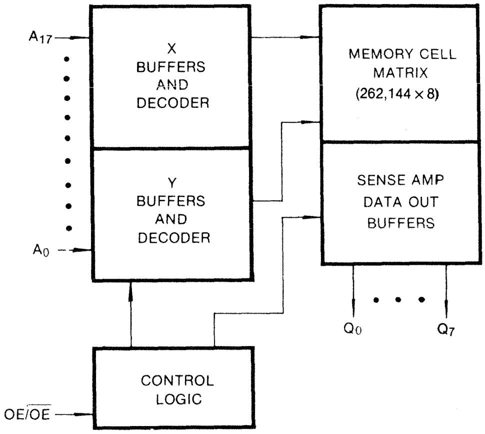
The KM23C2001 is a fully static mask programmable ROM organized 262,144 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

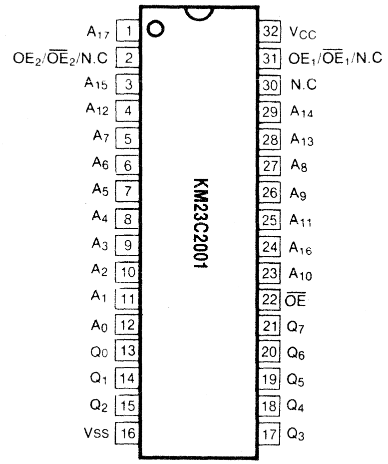
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C2001 is packaged in a 32-DIP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

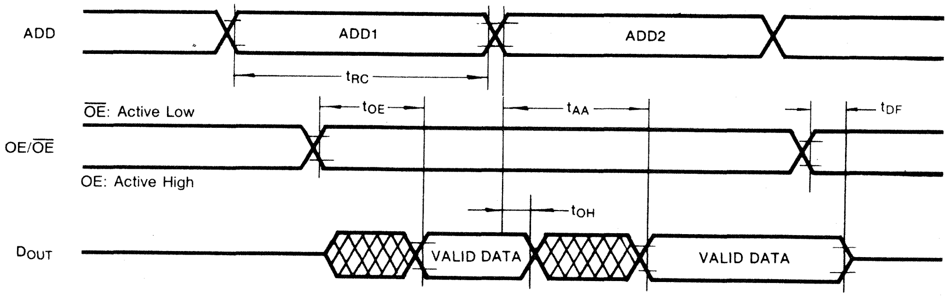
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2001-15		KM23C2001-20		KM23C2001-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

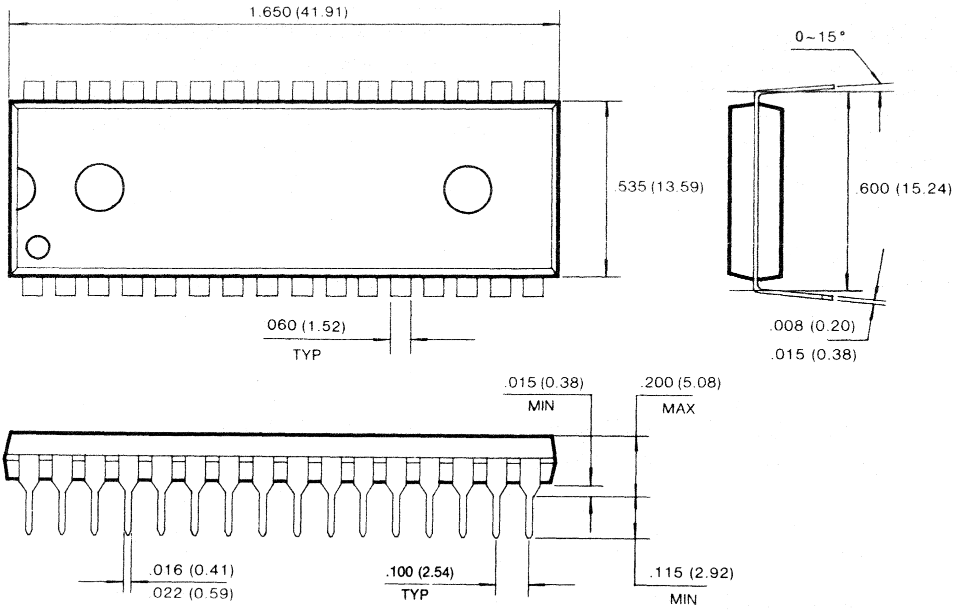
READ



PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2001)

Units: Inches (millimeters)



2M-Bit (256K × 8) CMOS MASK ROM

FEATURES

- **262,144 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 40mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**

GENERAL DESCRIPTION

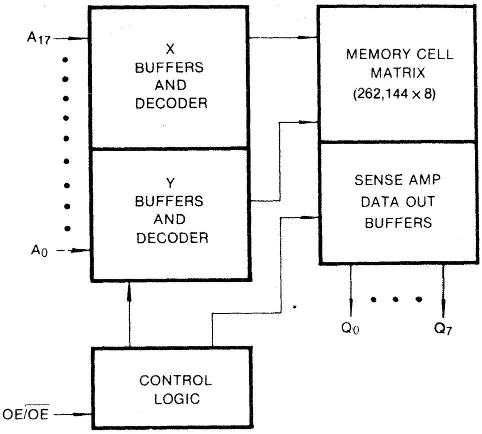
The KM23C2001H is a fully static mask programmable ROM organized 262,144 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

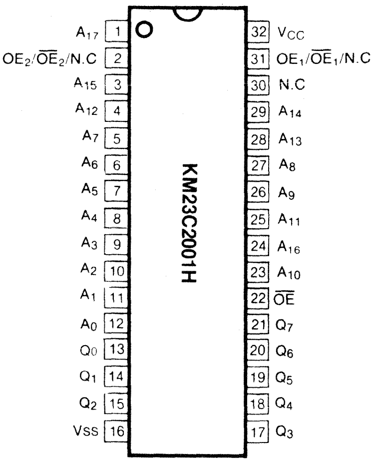
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C2001H is packaged in a 32-DIP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	40	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

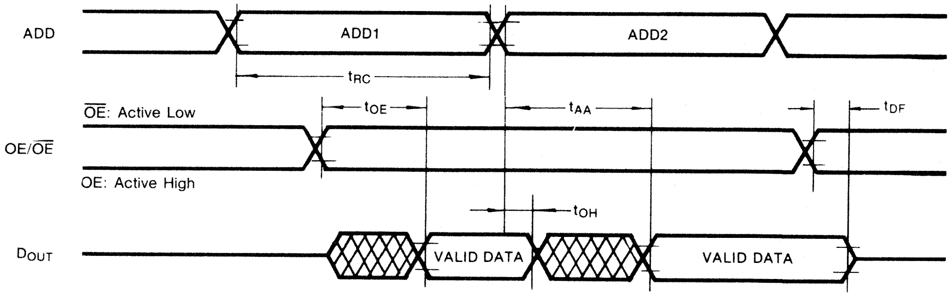
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2001H-10		KM23C2001H-12		KM23C2001H-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

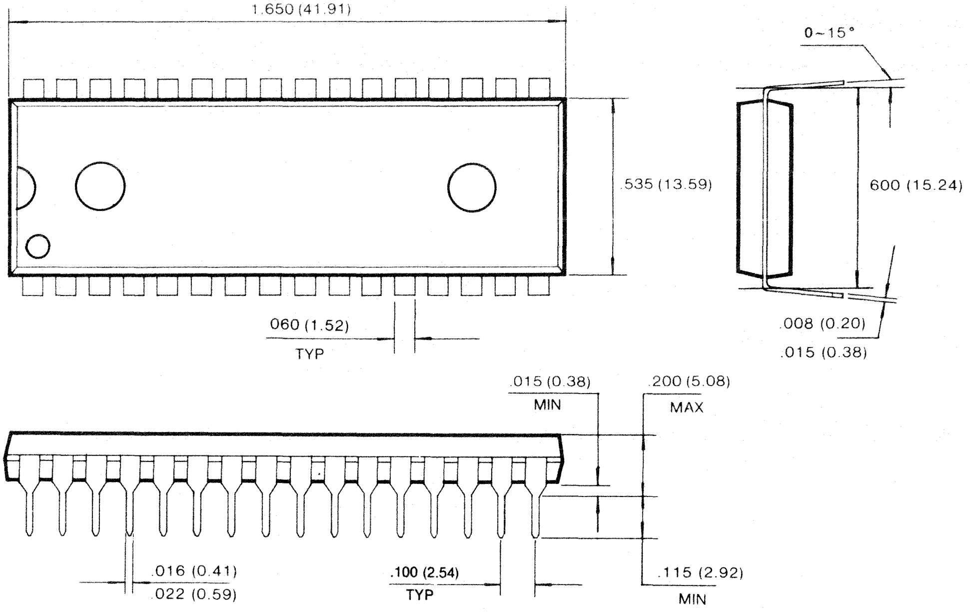
READ



PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2001H)

Units: Inches (millimeters)



2M-Bit (256K × 8/128K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 262,144 × 8
  Word Mode: 131,072 × 16
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP

GENERAL DESCRIPTION

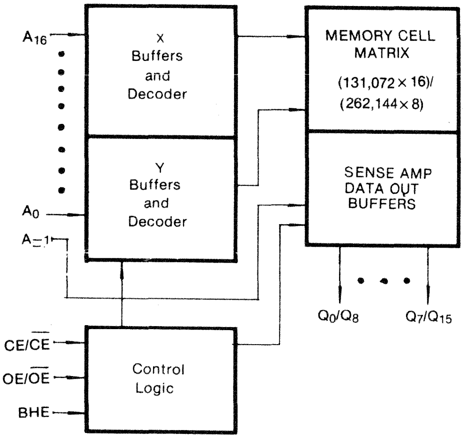
The KM23C2100 is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 262,144 × 8 bit (byte mode) or as 131,072 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

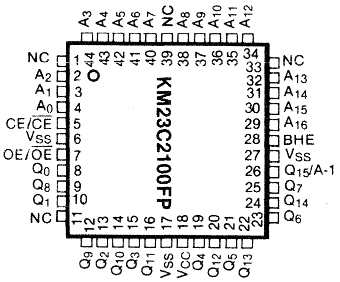
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

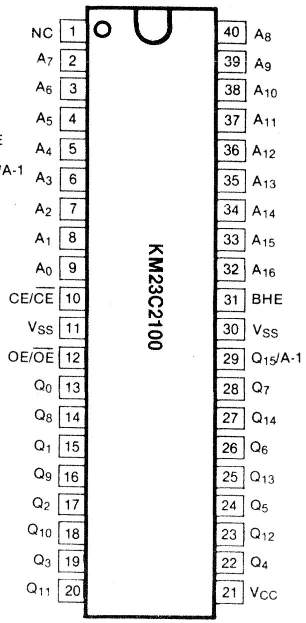
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C2100 is packaged in a 40-DIP, and the KM23C2100FP in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM







Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
$CE/\overline{CE}$*	Chip Enable
$OE/\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

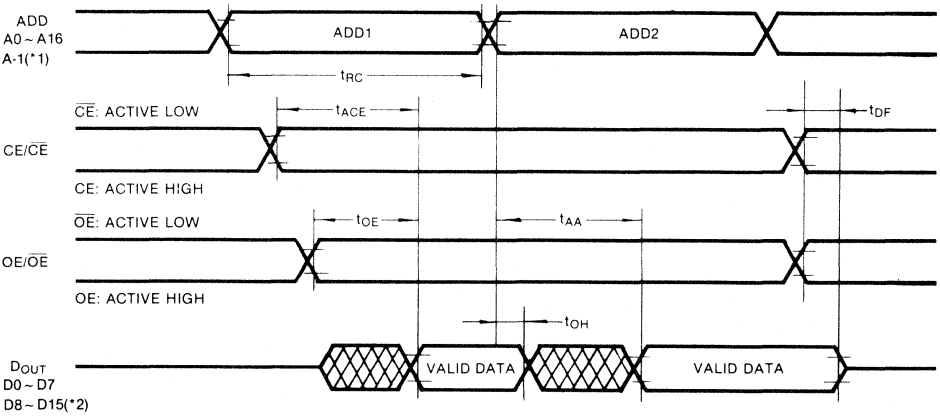
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2100(FP)-15		KM23C2100(FP)-20		KM23C2100(FP)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

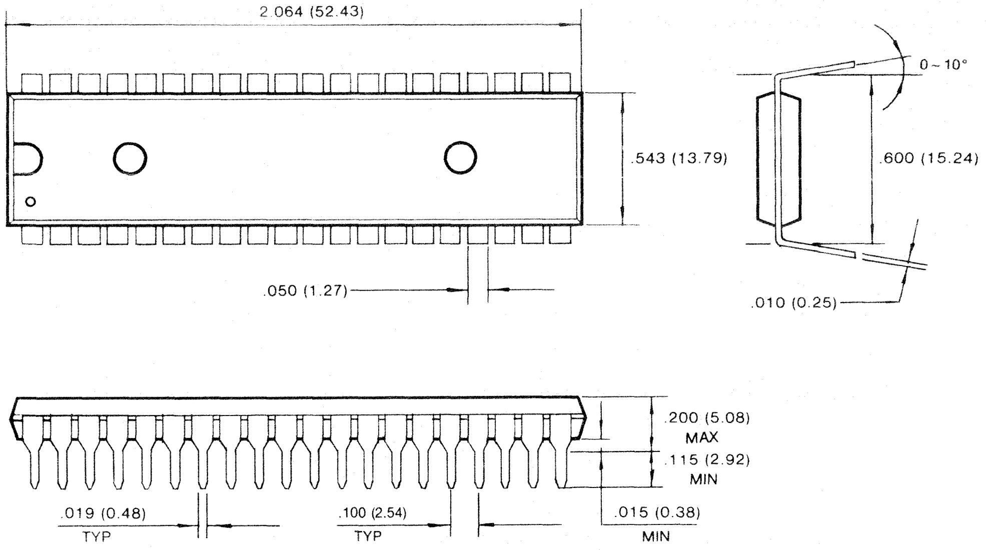


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

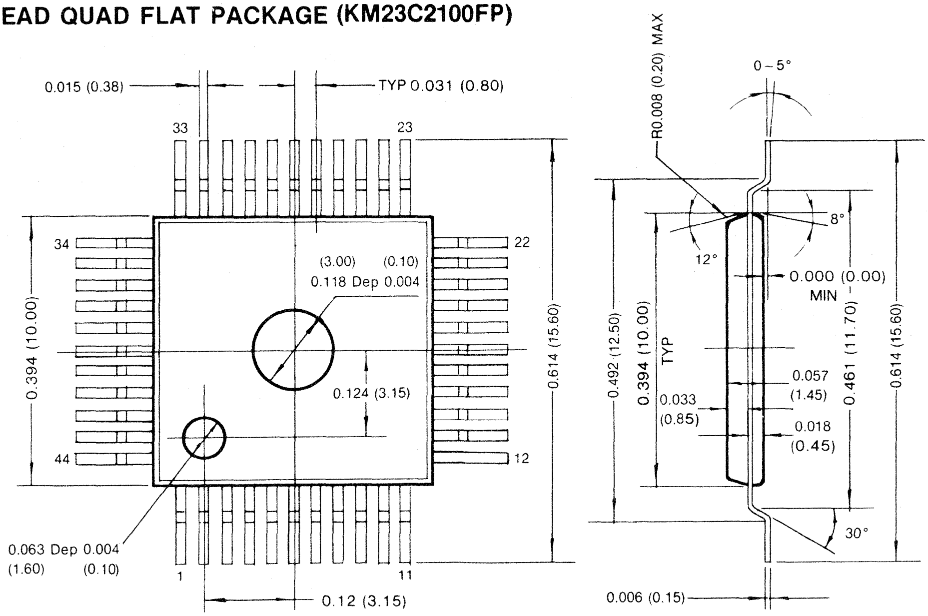
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2100)

Units: Inches (millimeters)



44 LEAD QUAD FLAT PACKAGE (KM23C2100FP)



2M-Bit (256K × 8/128K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 262,144 × 8
  Word Mode: 131,072 × 16
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP

GENERAL DESCRIPTION

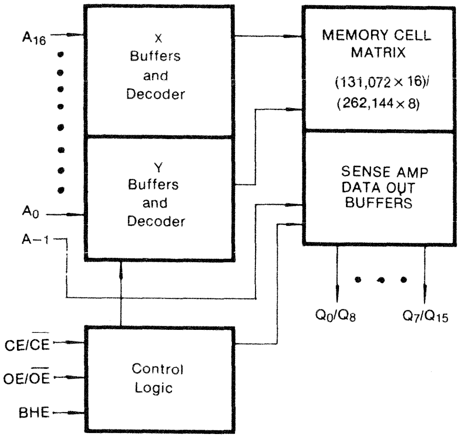
The KM23C2100H is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 262,144 × 8 bit (byte mode) or as 131,072 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

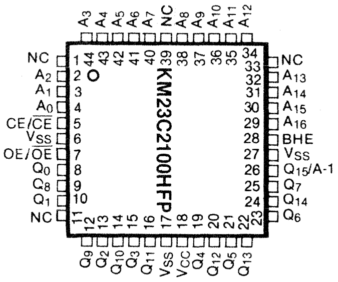
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

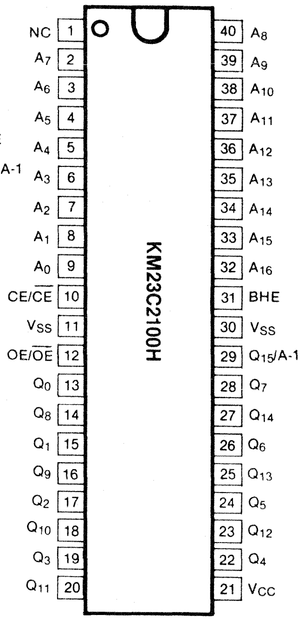
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C2100H is packaged in a 40-DIP, and the KM23C2100HFP in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM







Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $f = 5.0MHz$ all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, $f = 1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A_{-1}	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

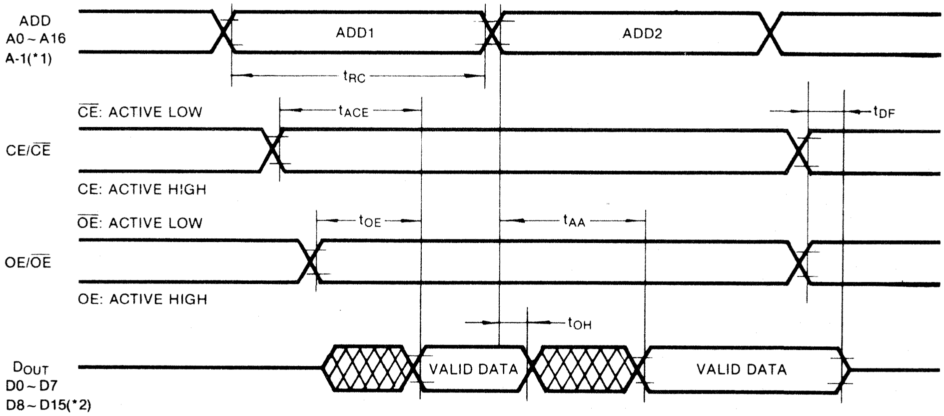
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2100H(FP)-10		KM23C2100H(FP)-12		KM23C2100H(FP)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

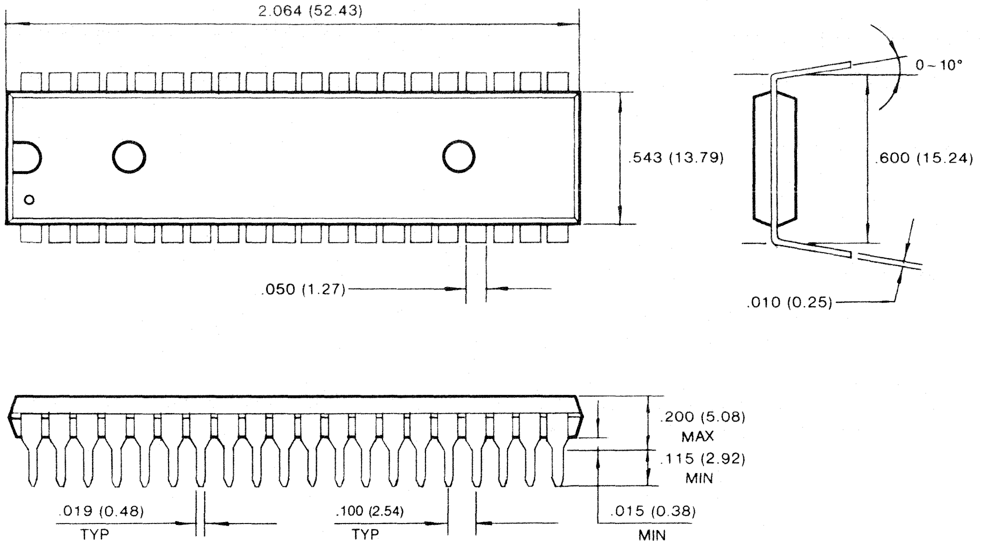


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

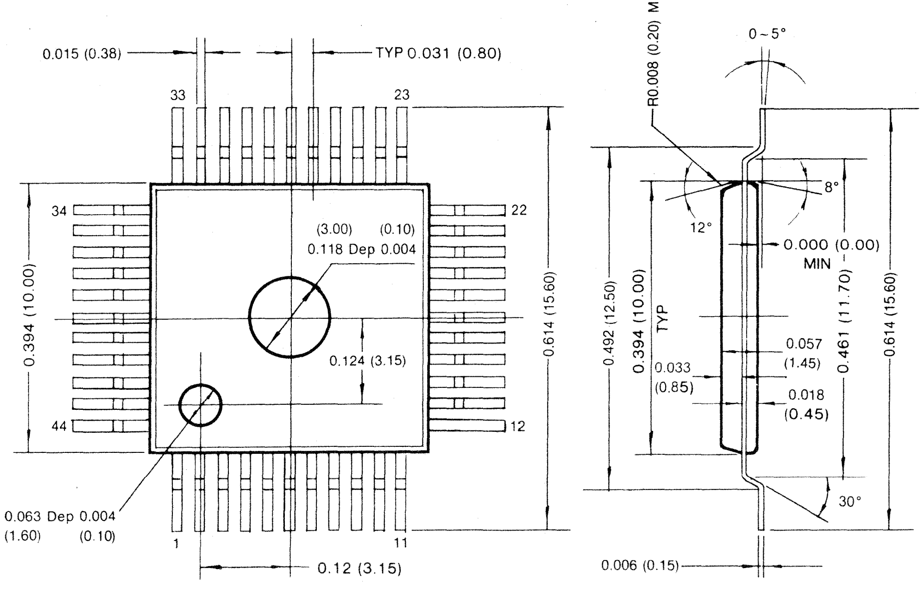
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2100H)

Units: Inches (millimeters)



44 LEAD QUAD FLAT PACKAGE (KM23C2100HFP)



4M-Bit (512K × 8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC Standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

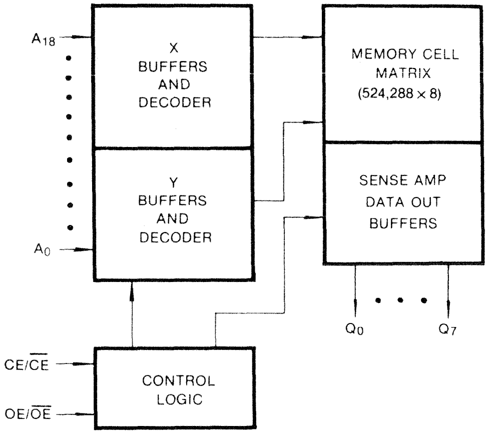
The KM23C4000A is a fully static mask programmable ROM organized 524,288×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

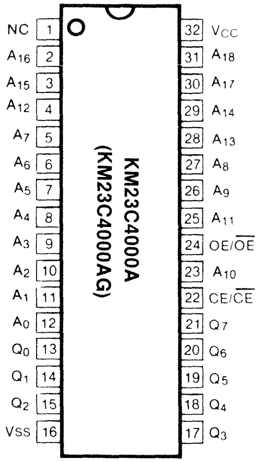
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C4000A is packaged in a 32-DIP, and the KM23C4000AG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	$f = 6.7MHz$	—	50	mA
	I_{CC2}		$f = 1.0MHz$	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25°C$, $f = 1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

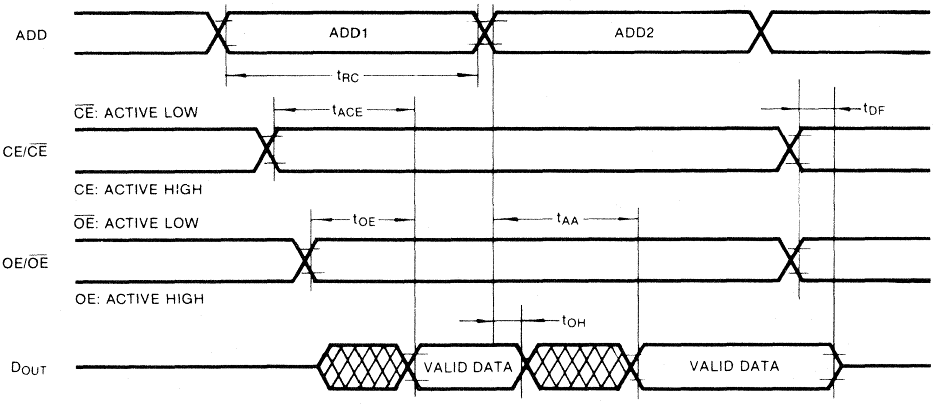
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4000A(G)-15		KM23C4000A(G)-20		KM23C4000A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}				90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}				70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

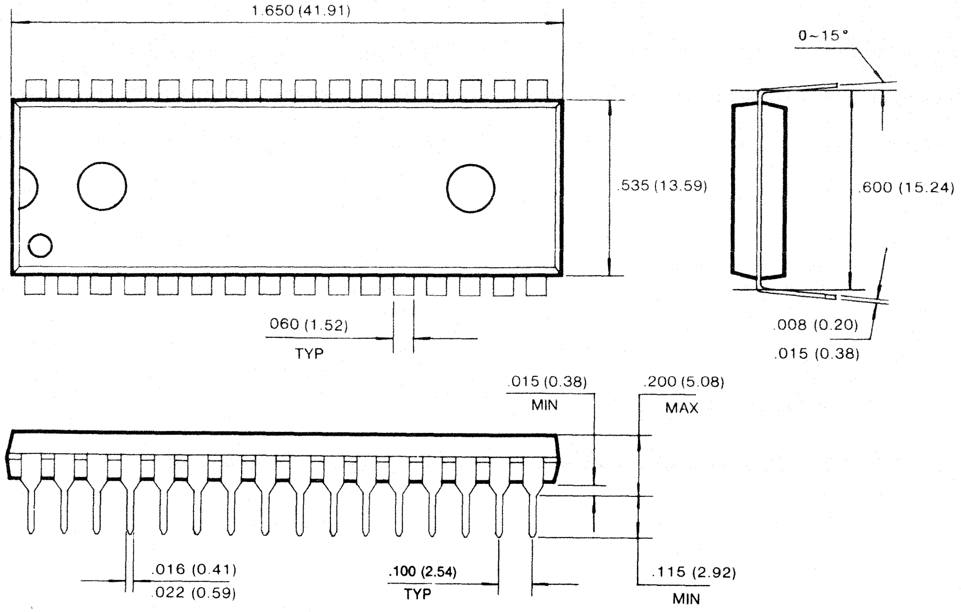


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

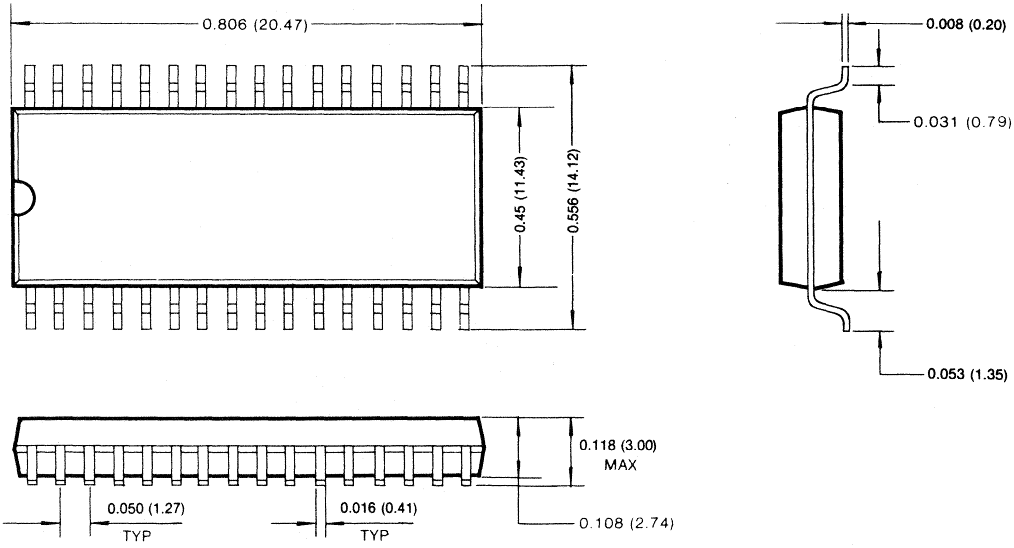
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4000A)

Units: inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4000AG)



4M-Bit (512K × 8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

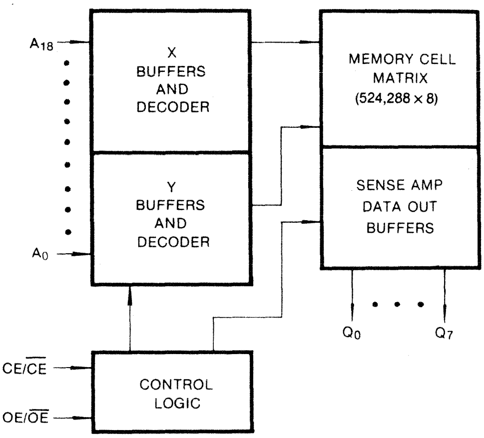
The KM23C4000B is a fully static mask programmable ROM organized 524,288 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

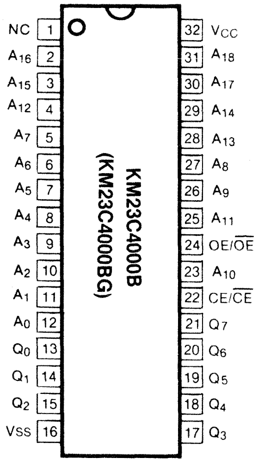
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4000B is packaged in a 32-DIP, and the KM23C4000BG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
$CE/\overline{CE}$*	Chip Enable
$OE/\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	$f=6.7MHz$	—	50	mA
	I_{CC2}		$f=1.0MHz$	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE ($T_A=25$°C, $f=1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

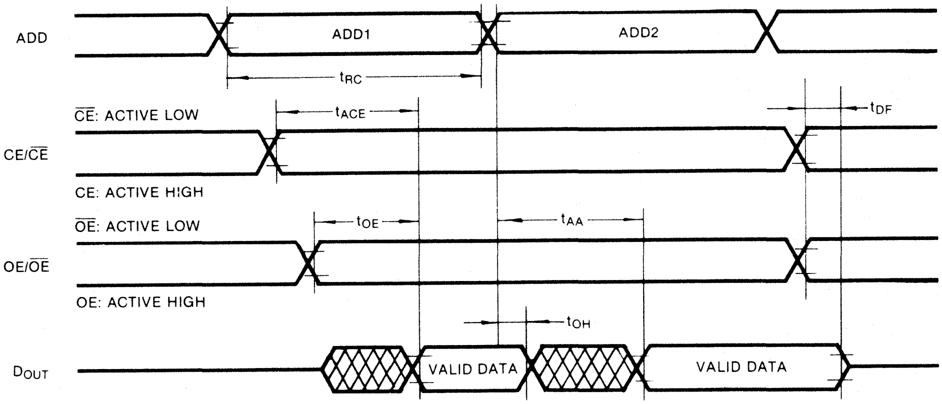
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4000B(G)-12		KM23C4000B(G)-15		KM23C4000B(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

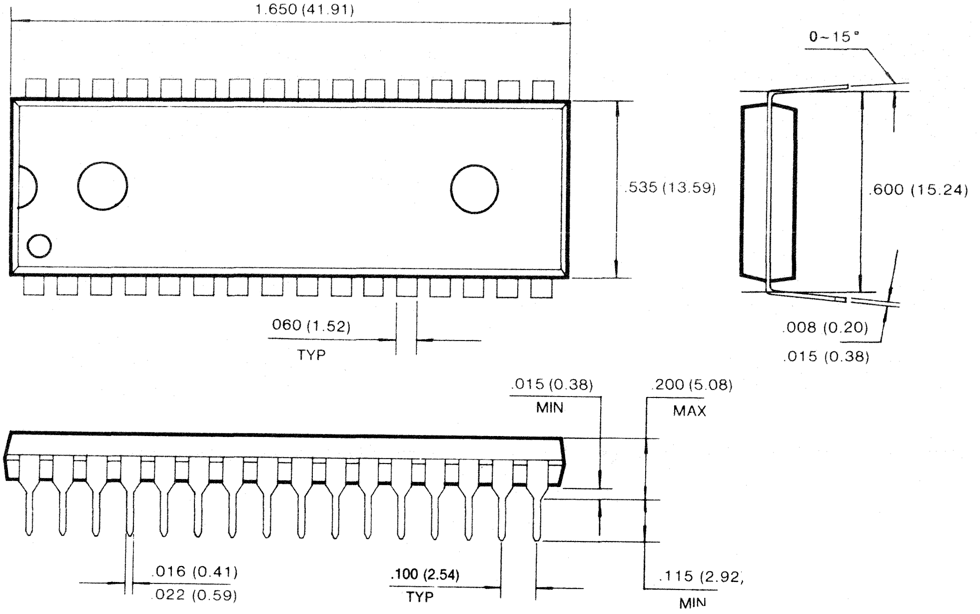


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

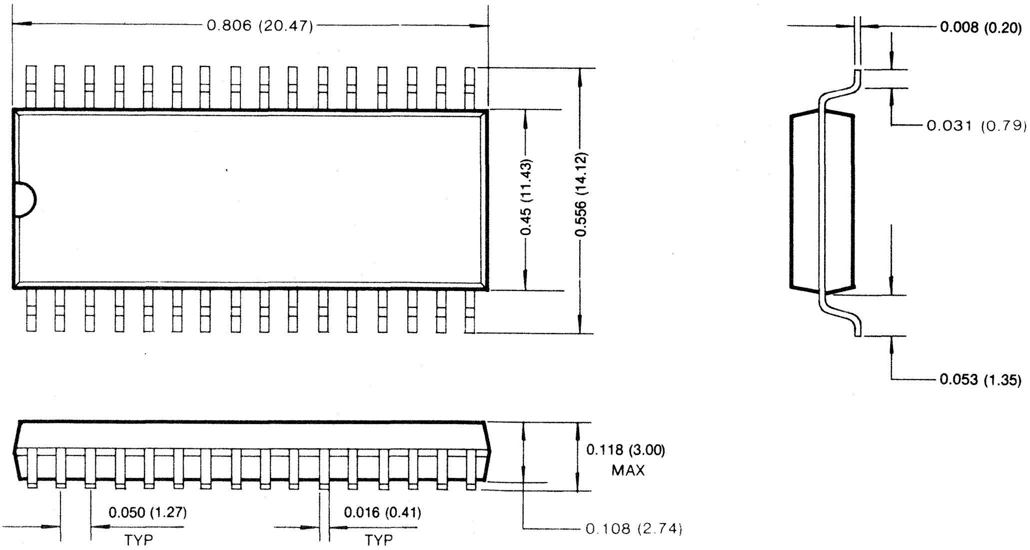
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4000B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4000BG)



4M-Bit (512K × 8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC Standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

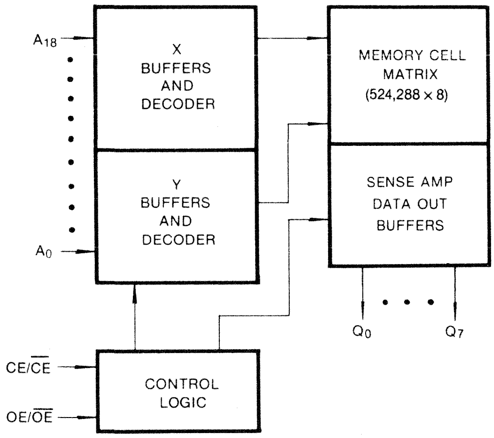
The KM23C4000H is a fully static mask programmable ROM organized 524,288 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

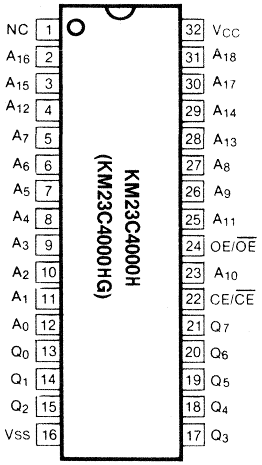
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4000H is packaged in a 32-DIP, and the KM23C4000HG packaged in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	$f = 6.7MHz$	—	50	mA
	I_{CC2}		$f = 1.0MHz$	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25°C$, $f = 1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

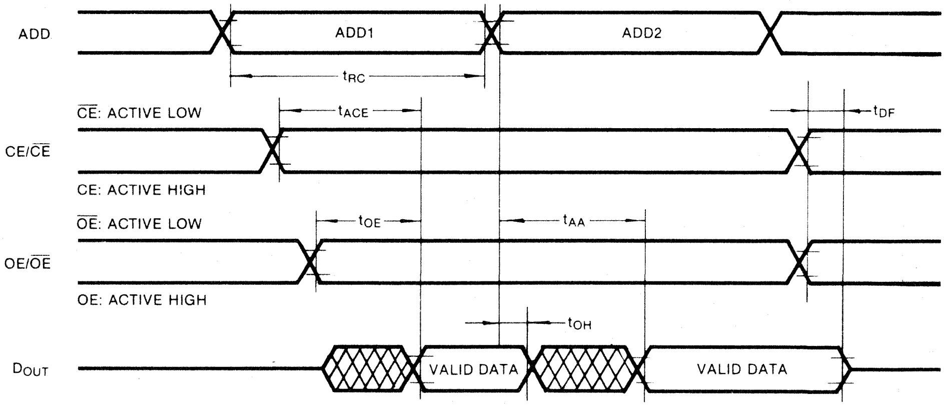
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4000H(G)-10		KM23C4000H(G)-12		KM23C4000H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

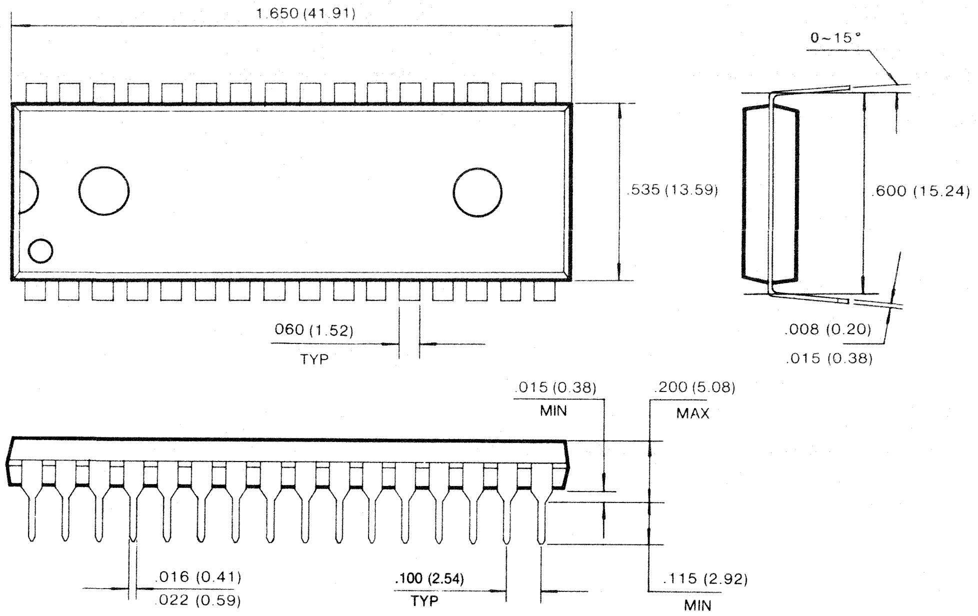


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

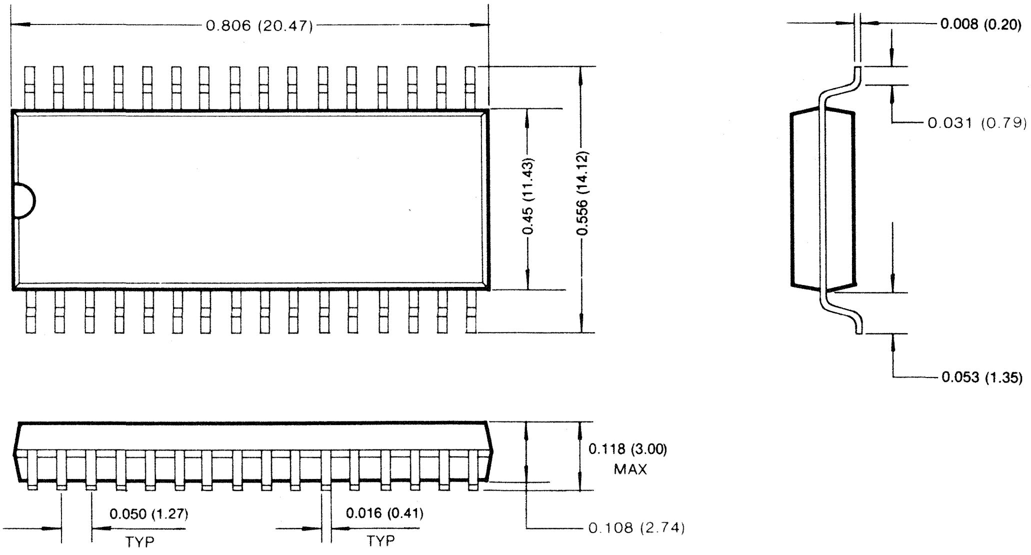
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4000H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4000HG)



4M-Bit (512K×8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**

  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

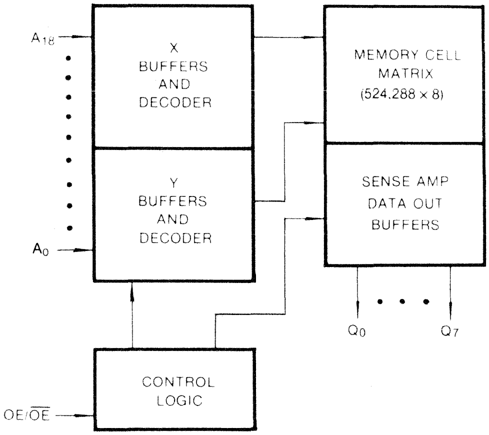
The KM23C4001A is a fully static mask programmable ROM organized 524,288×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

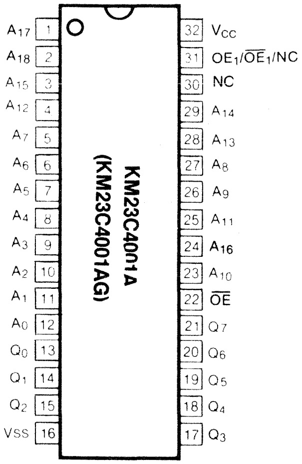
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4001A is packaged in a 32-DIP and the KM23C4001AG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

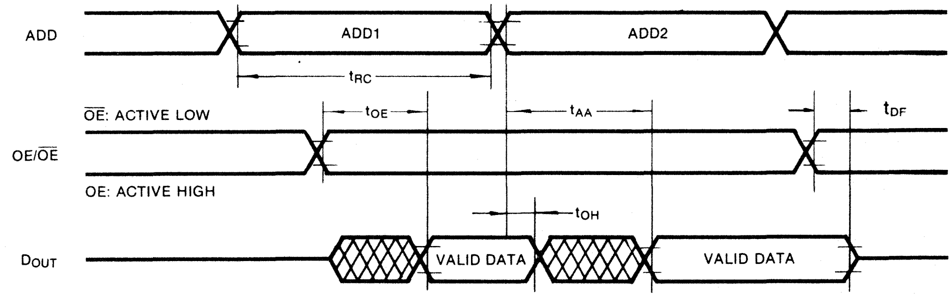
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C4001A(G)-15		KM23C4001A(G)-20		KM23C4001A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

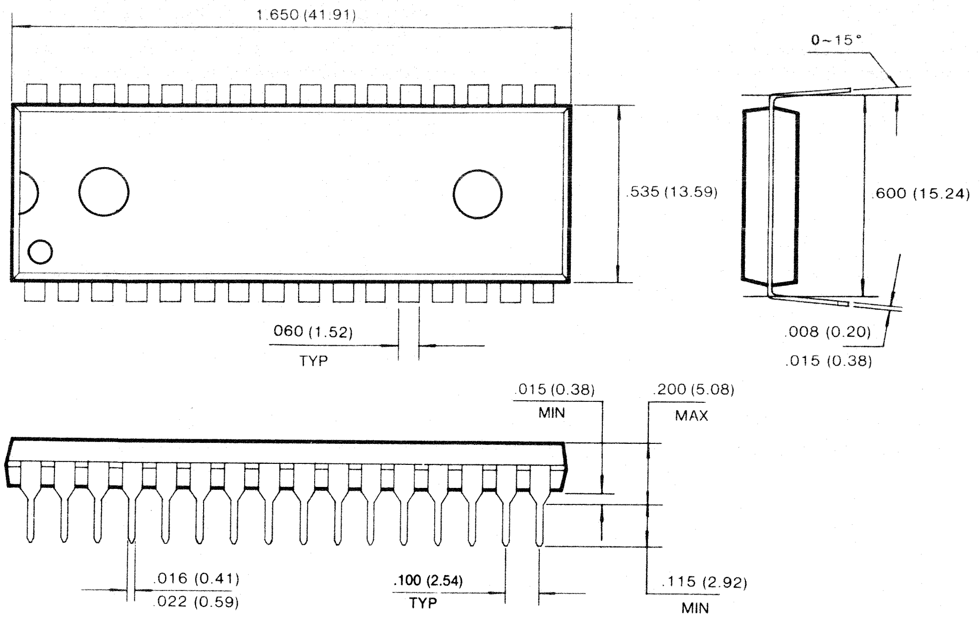
READ



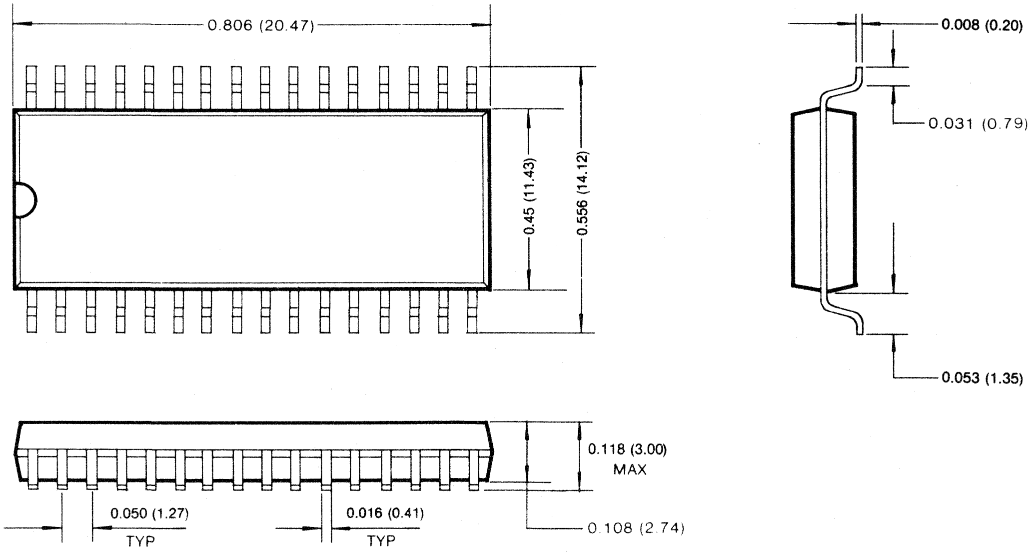
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4001A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4001AG)



4M-Bit (512K×8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**

  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

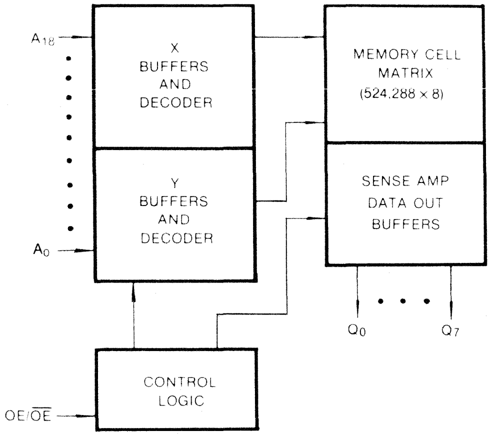
The KM23C4001B is a fully static mask programmable ROM organized 524,288×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

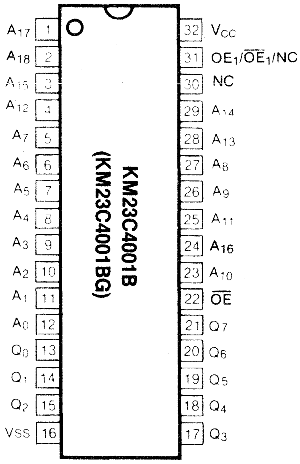
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4001B is packaged in a 32-DIP and the KM23C4001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

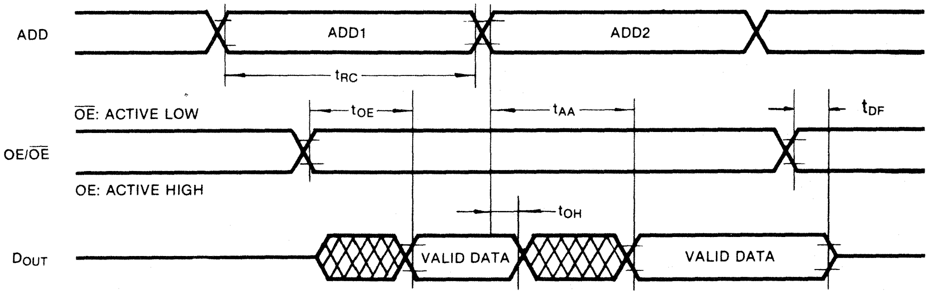
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4001B(G)-12		KM23C4001B(G)-15		KM23C4001B(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

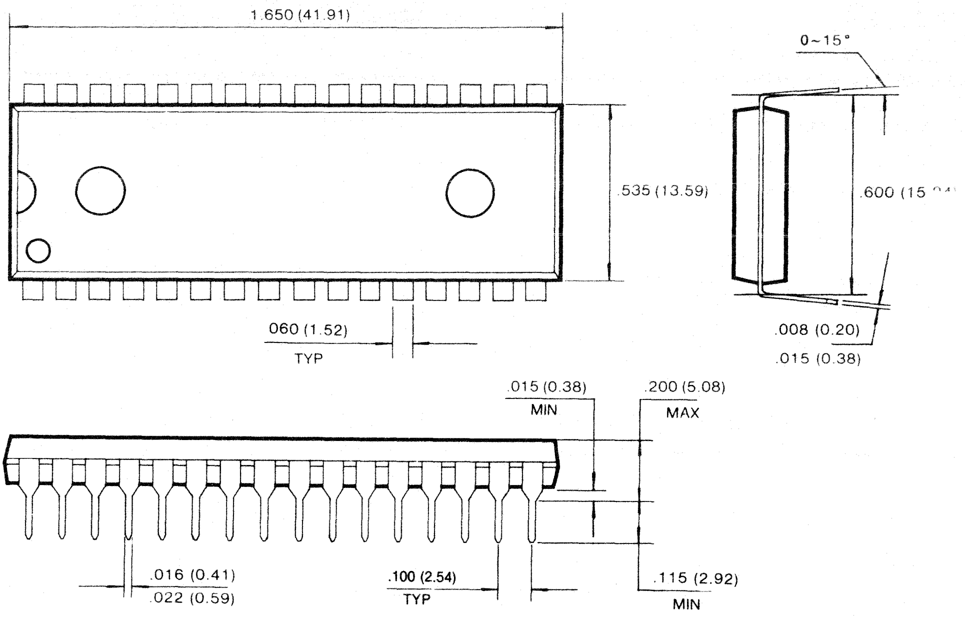
READ



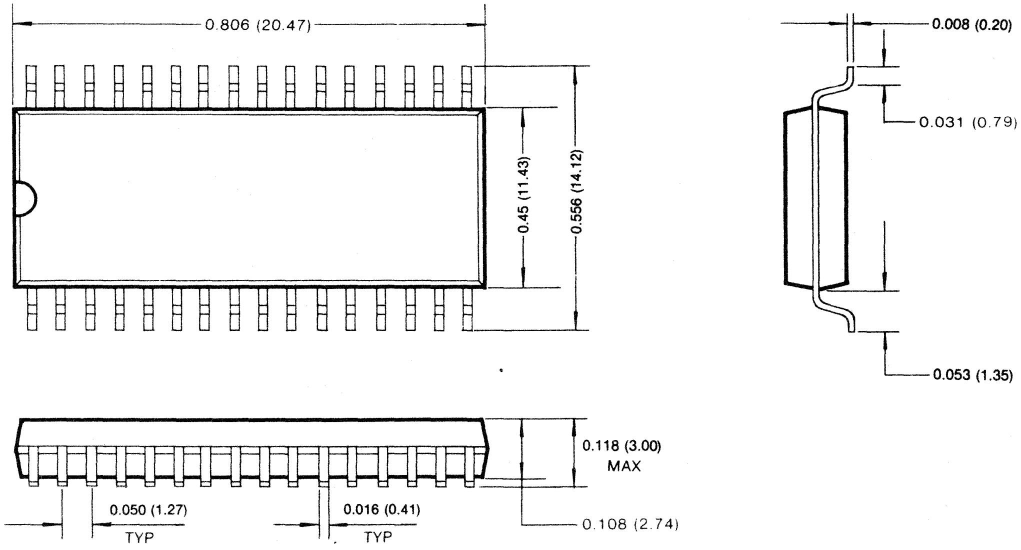
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4001B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4001BG)



4M-Bit (512K × 8) CMOS MASK ROM

FEATURES

- **524,288 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**

  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

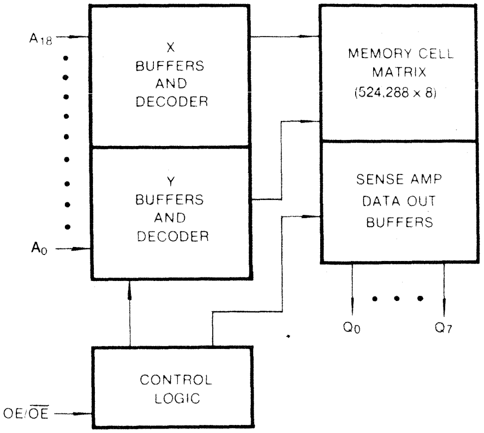
The KM23C4001H is a fully static mask programmable ROM organized 524,288×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

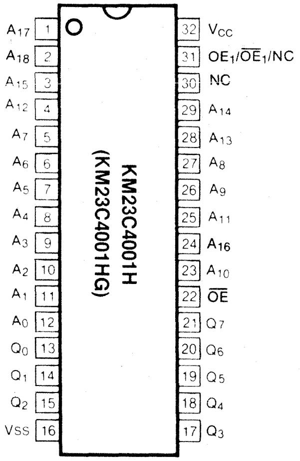
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4001H is packaged in a 32-DIP and the KM23C4001HG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A=0°C$ to $+70°C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted.)

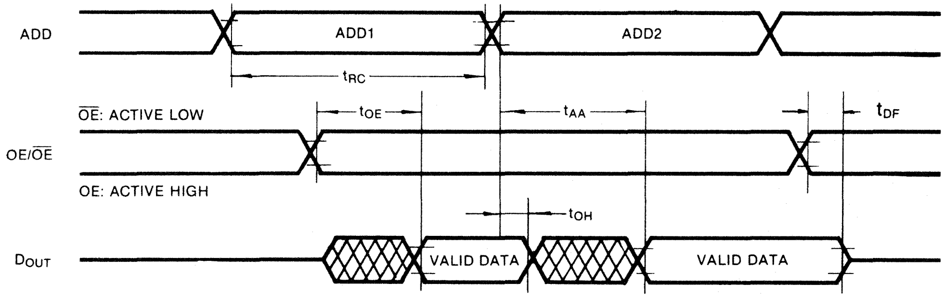
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4001H(G)-10		KM23C4001H(G)-12		KM23C4001H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

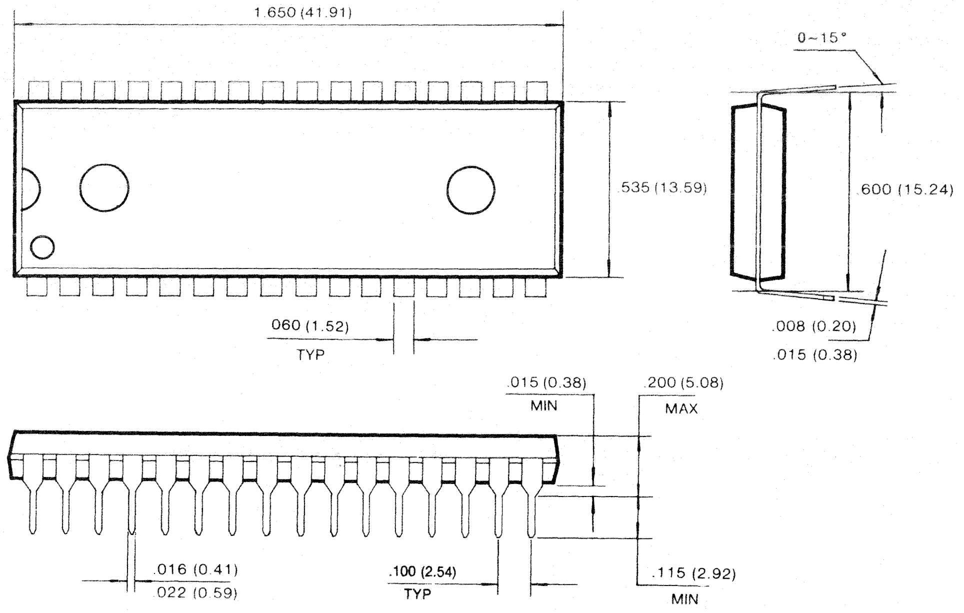
READ



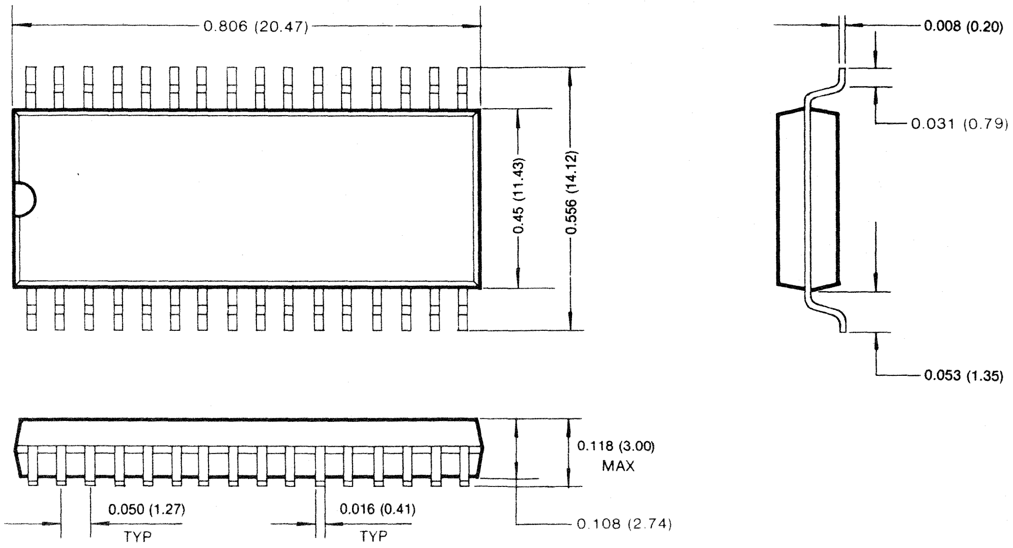
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4001H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4001HG)



KM23C4100AG CMOS MASK ROM

4M-Bit (512K × 8/256K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 × 8
  Word Mode: 262,144 × 16
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin 525 mil, plastic SOP**

GENERAL DESCRIPTION

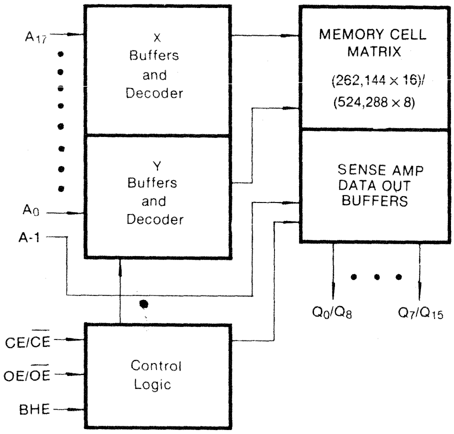
The KM23C4100AG is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 × 8 bit (byte mode) or as 262,144 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4100AG is packaged in a 40-SOP, provides polarity programmable CE and OE buffer as user option mode.

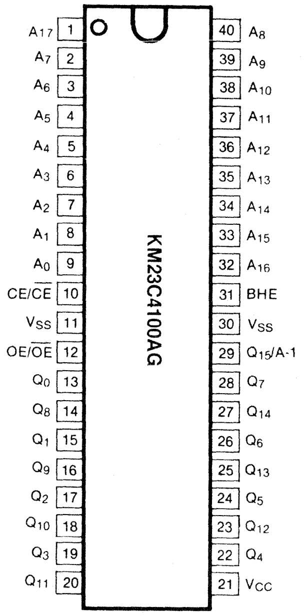
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

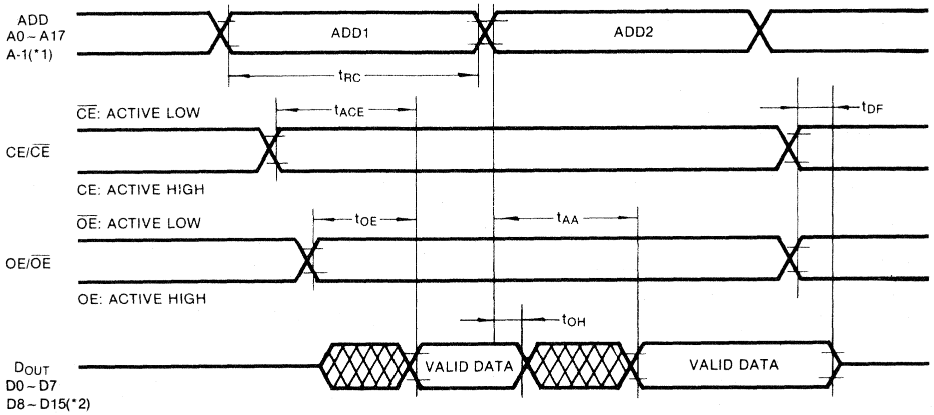
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4100AG-15		KM23C4100AG-20		KM23C4100AG-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



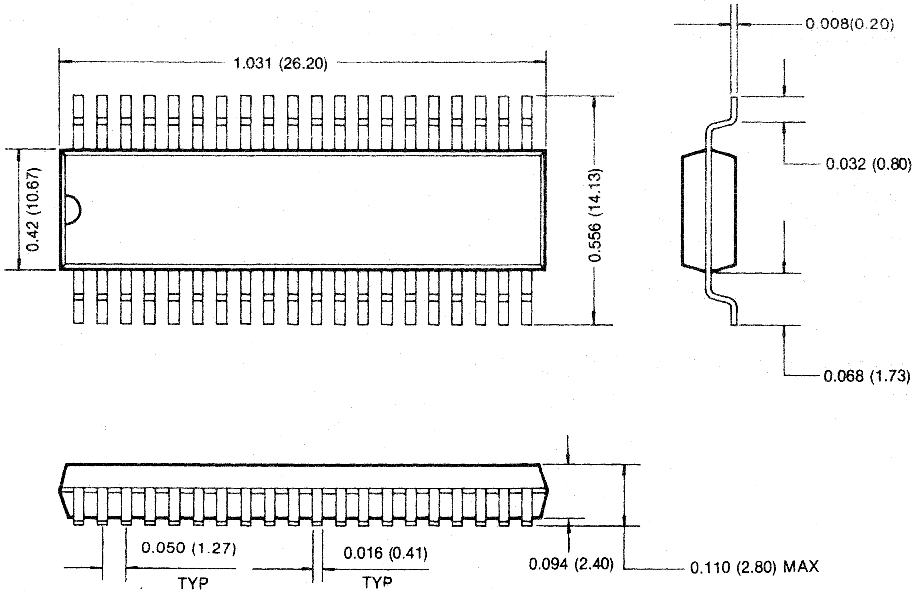
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

40 LEAD SMALL OUTLINE PACKAGE (KM23C4100AG)

Units: Inches (millimeters)

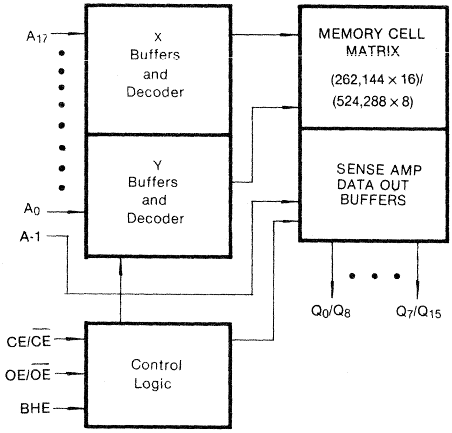


4M-Bit (512K × 8/256K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 × 8
  Word Mode: 262,144 × 16
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP (14 × 14) (10 × 10)

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

GENERAL DESCRIPTION

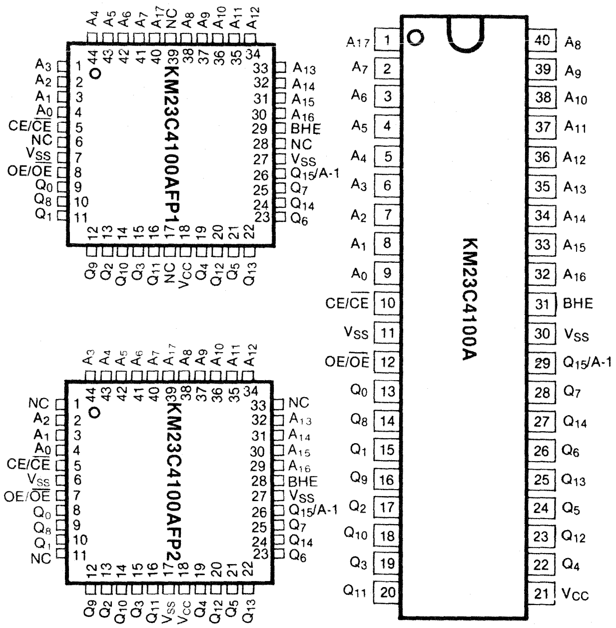
The KM23C4100A is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 × 8 bit (byte mode) or as 262,144 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4100A is packaged in a 40-DIP, and the KM23C4100AFP1, KM23C4100AFP2 in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	$f = 6.7MHz$	—	50	mA
	I_{CC2}		$f = 1.0MHz$	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

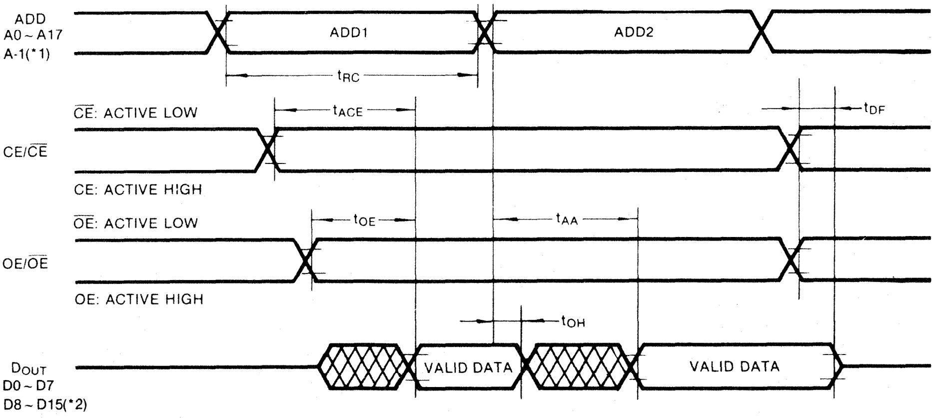
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4100A(FP)-15		KM23C4100A(FP)-20		KM23C4100A(FP)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



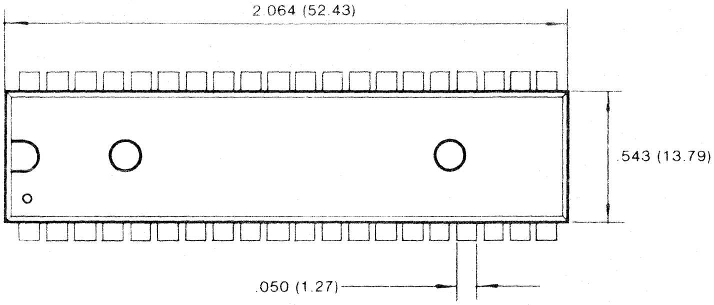
(*1) Byte Mode only. A-1 is Least Significant Bit Address. ($BHE = V_{IL}$)
(*2) Word Mode only. ($BHE = V_{IH}$)

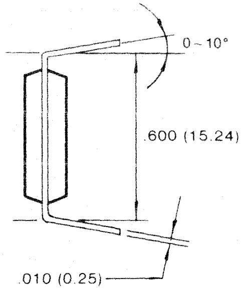
* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

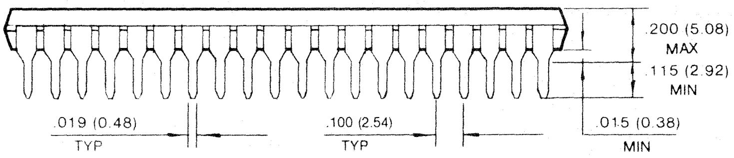
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4100A)

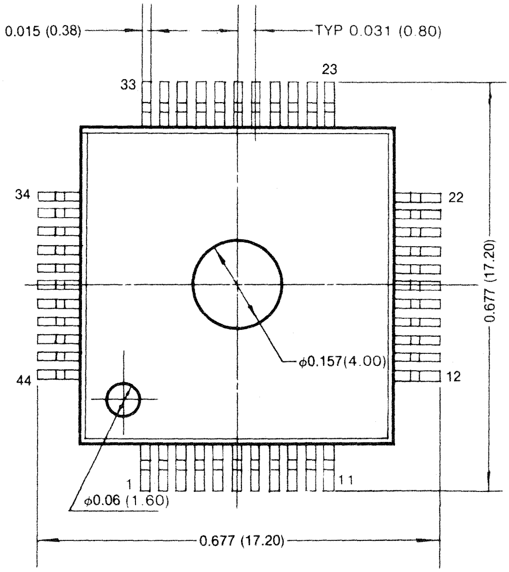
Units: Inches (millimeters)

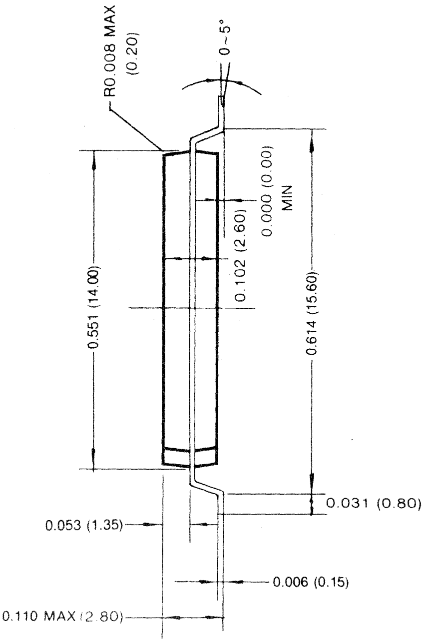






44 LEAD QUAD FLAT PACKAGE (KM23C4100AFP1)

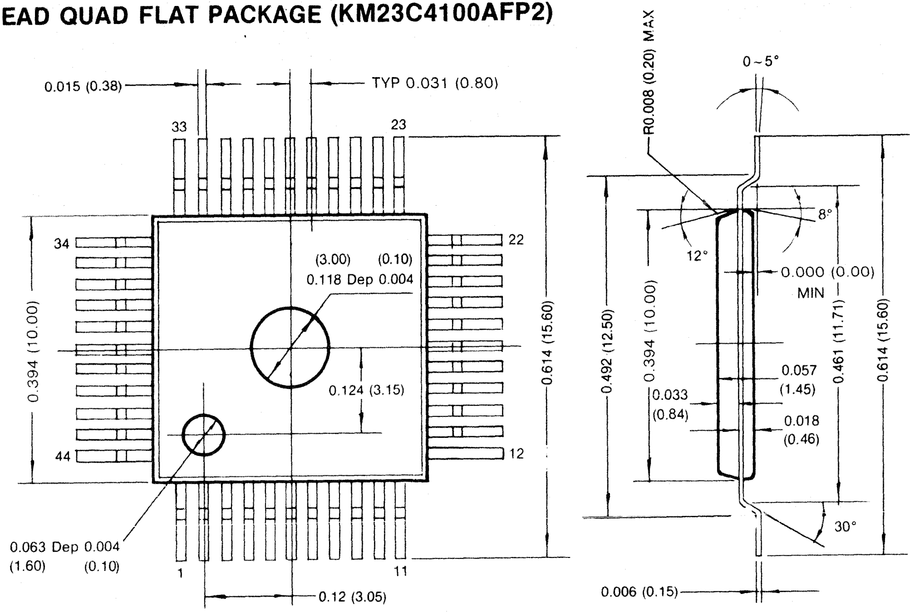




PACKAGE DIMENSIONS (Continued)

Units: Inches (millimeters)

44 LEAD QUAD FLAT PACKAGE (KM23C4100AFP2)



4M-Bit (512K × 8/256K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 × 8
  Word Mode: 262,144 × 16
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP (14 × 14) (10 × 10)

GENERAL DESCRIPTION

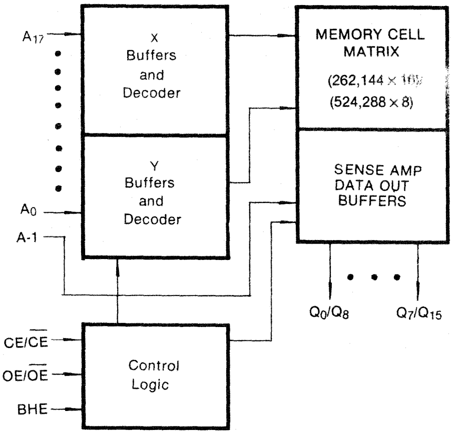
The KM23C4100B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 × 8 bit (byte mode) or as 262,144 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

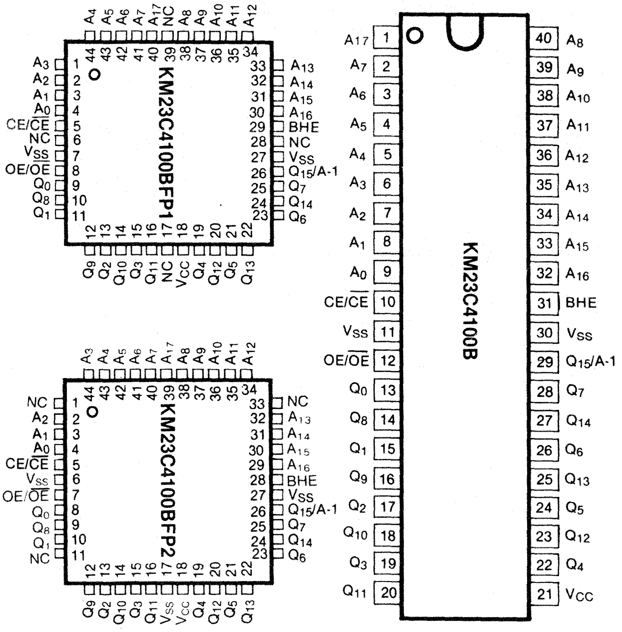
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4100B is packaged in a 40-DIP, and the KM23C4100BFP1, KM23C4100BFP2 in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, [illegible]MHz	—	50	mA
	I_{CC2}	all output open [illegible]z	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all out[illegible] open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, $f = 1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

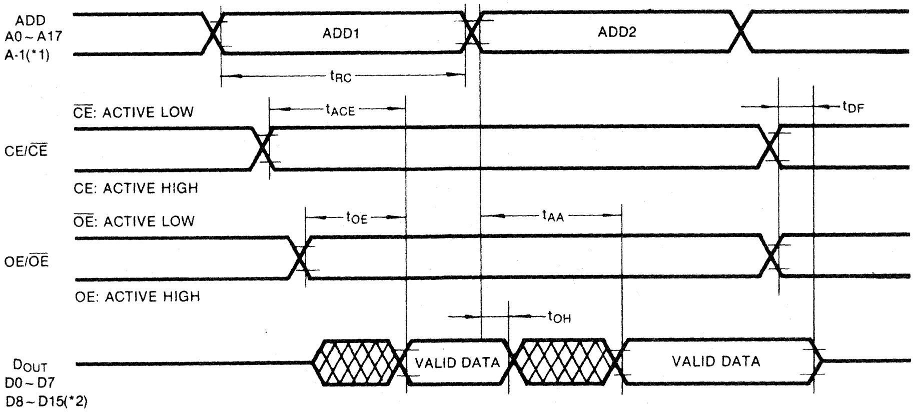
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4100B(FP)-12		KM23C4100B(FP)-15		KM23C4100B(FP)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



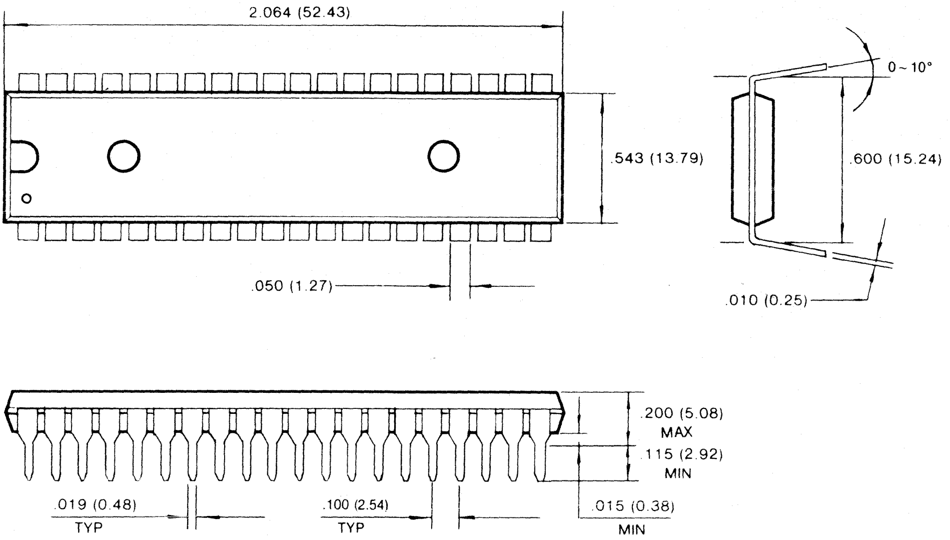
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

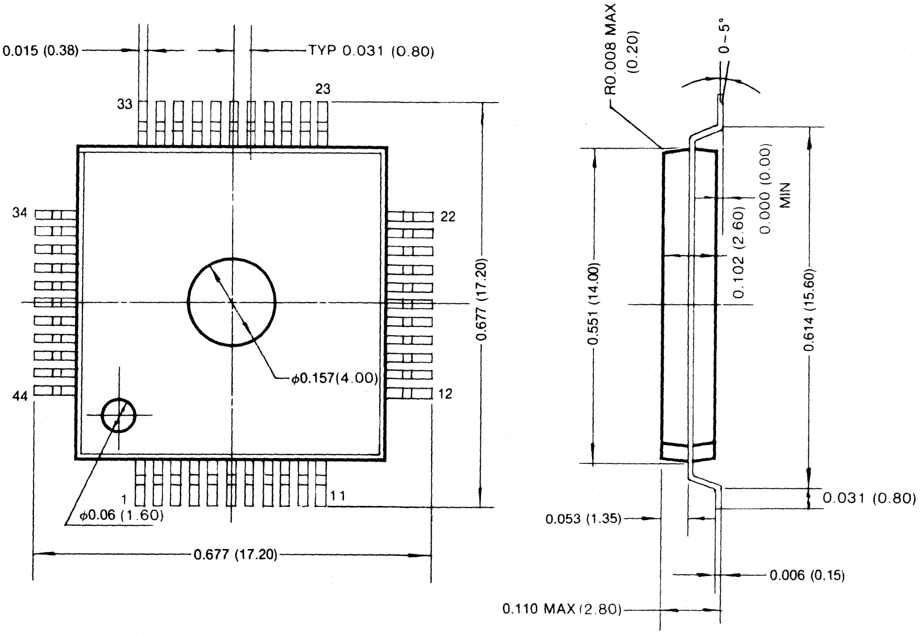
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4100B)

Units: Inches (millimeters)



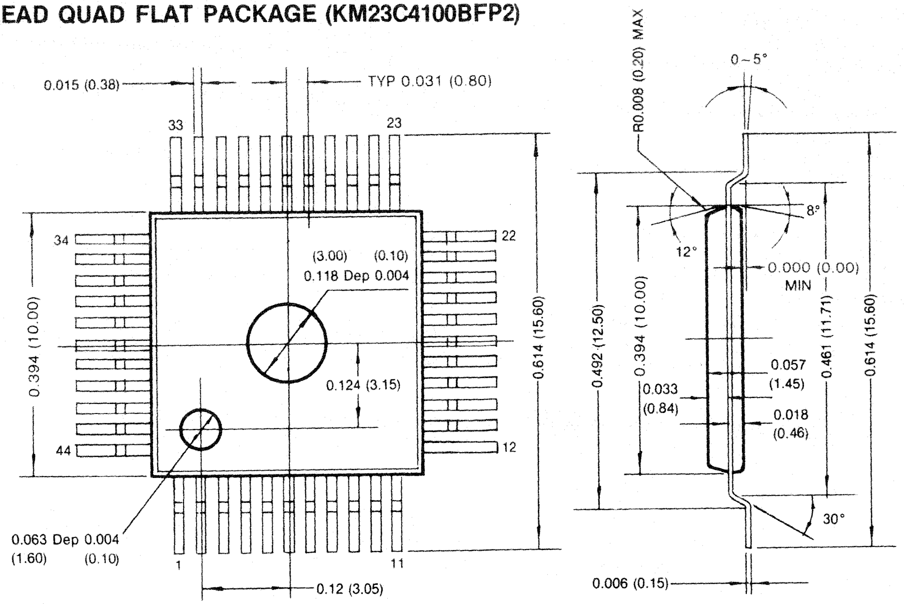
44 LEAD QUAD FLAT PACKAGE (KM23C4100BFP1)



PACKAGE DIMENSIONS (Continued)

44 LEAD QUAD FLAT PACKAGE (KM23C4100BFP2)

Units: Inches (millimeters)



4M-Bit (512K x 8/256K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 x 8
  Word Mode: 262,144 x 16
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP (14 x 14) (10 x 10)

GENERAL DESCRIPTION

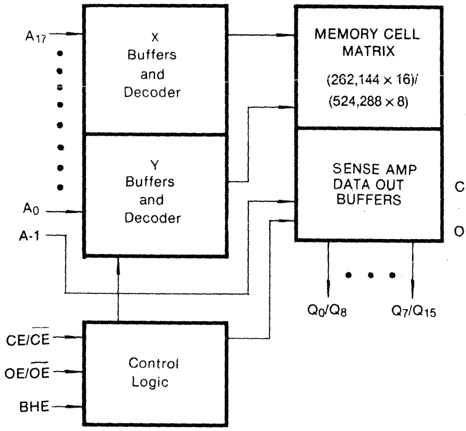
The KM23C4100H is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 x 8 bit (byte mode) or as 262,144 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4100H is packaged in a 40-DIP, and the KM23C4100HFP in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

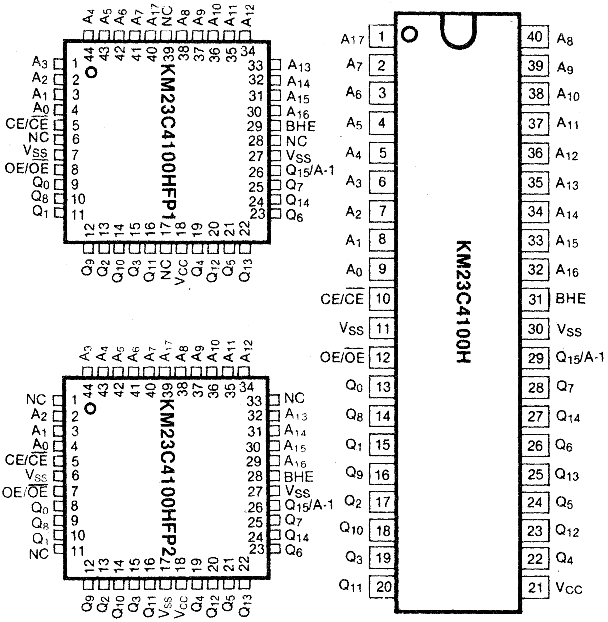
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to $+7.0$	V
Temperature Under Bias	T_{bias}	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	$f=6.7MHz$	—	60	mA
	I_{CC2}		$f=1.0MHz$	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE ($T_A=25°C$, $f=1.0MHz$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

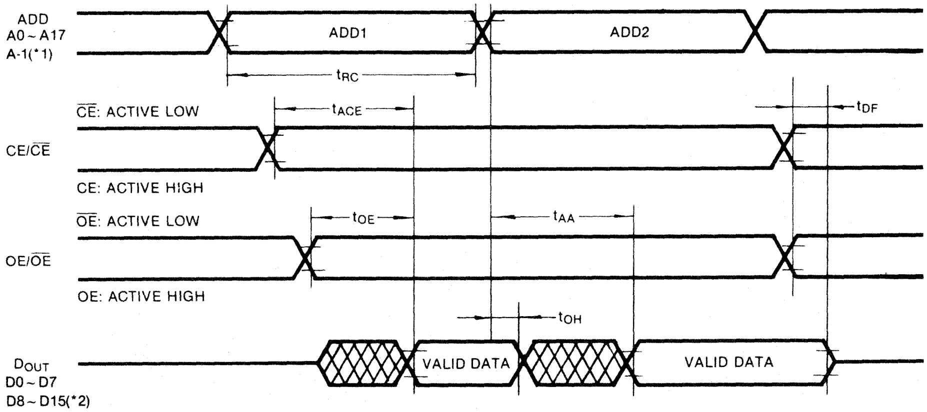
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4100H(FP)-10		KM23C4100H(FP)-12		KM23C4100H(FP)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



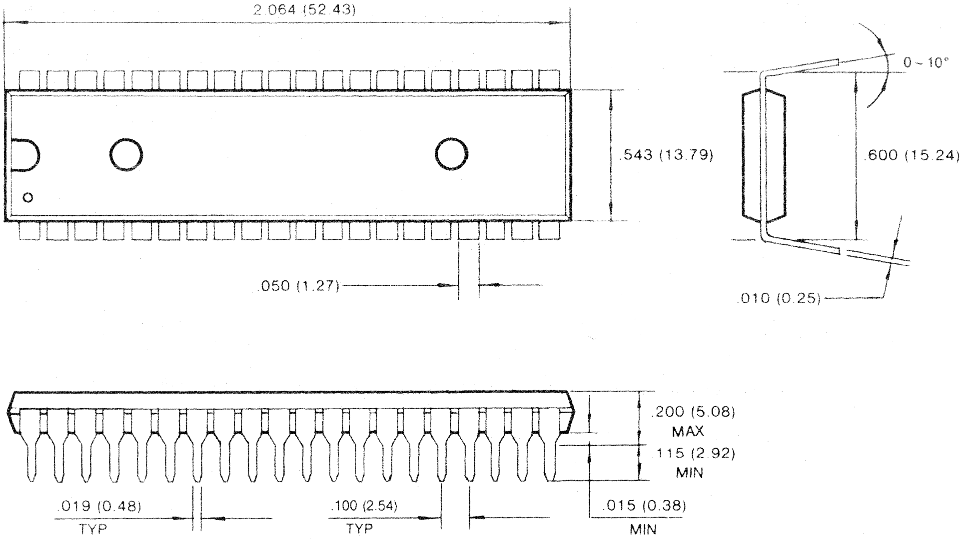
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

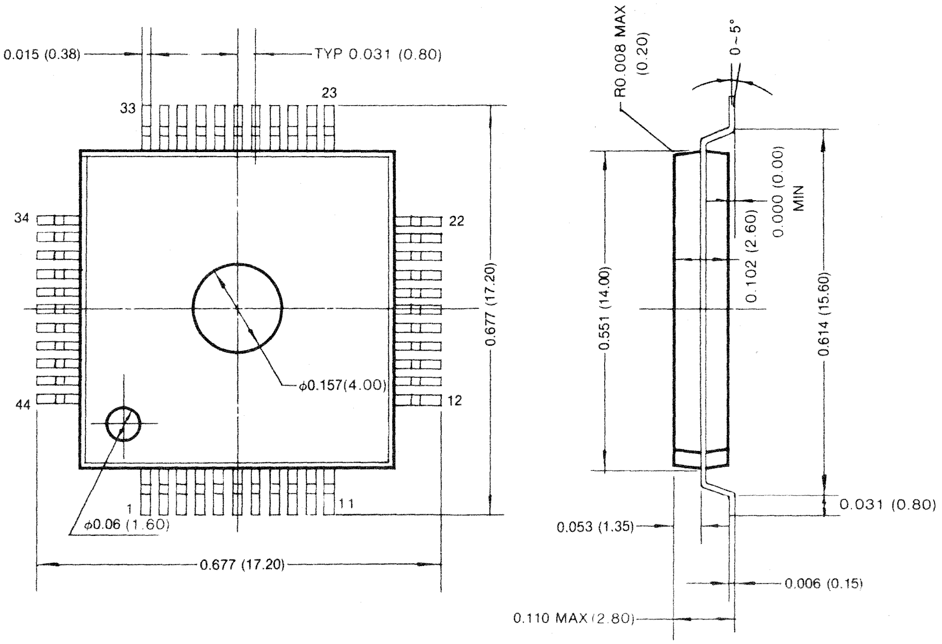
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4100H)

Units: Inches (millimeters)



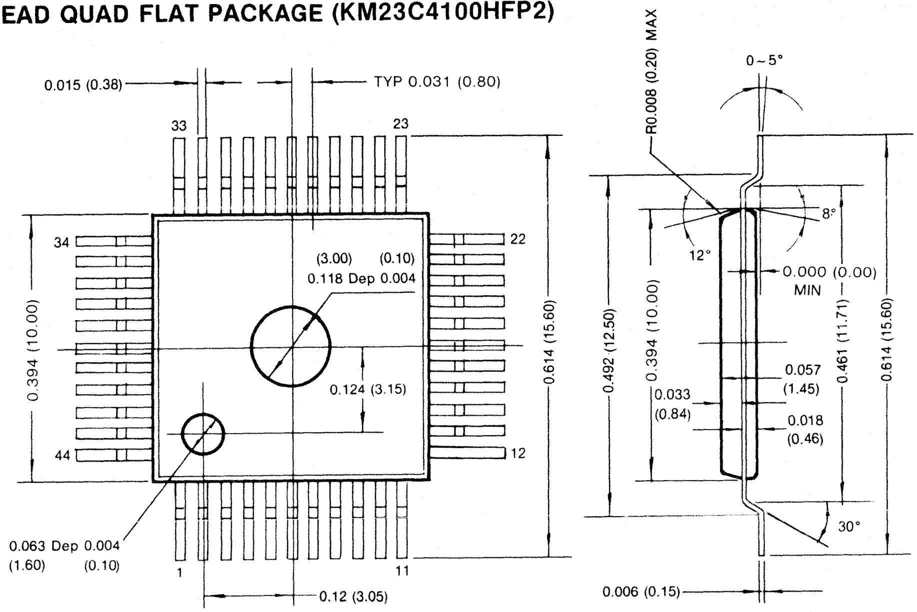
44 LEAD QUAD FLAT PACKAGE (KM23C4100HFP1)



PACKAGE DIMENSIONS (Continued)

Units: Inches (millimeters)

44 LEAD QUAD FLAT PACKAGE (KM23C4100HFP2)



4M-Bit (512K × 8/256K × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 × 8
  Word Mode: 262,144 × 16
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  (JEDEC Standard)

GENERAL DESCRIPTION

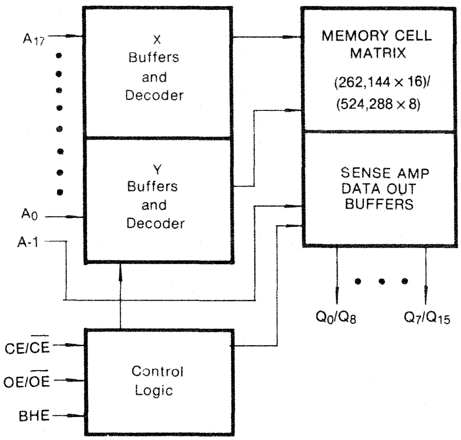
The KM23C4200B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 × 8 bit (byte mode) or as 262,144 × 16 bit (word mode) depending on BHE (pin 1) voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

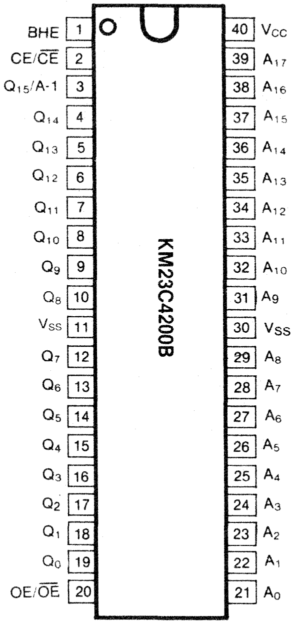
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4200B is packaged in a 40-DIP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_A = 25$°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

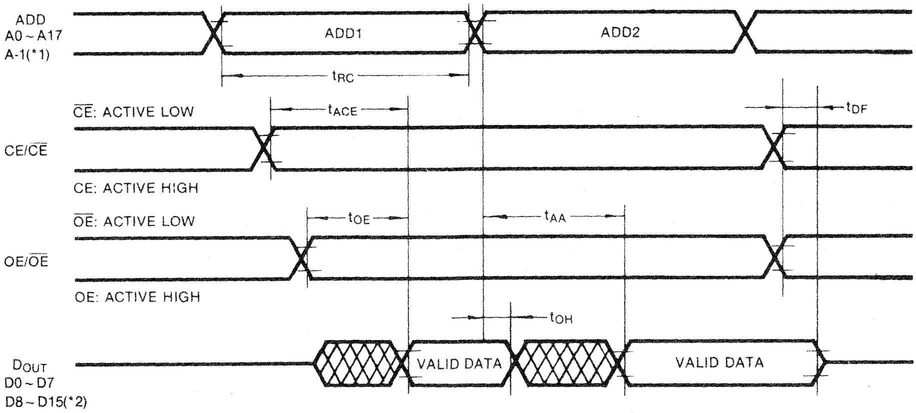
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C4200B-15		KM23C4200B-20		KM23C4200B-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



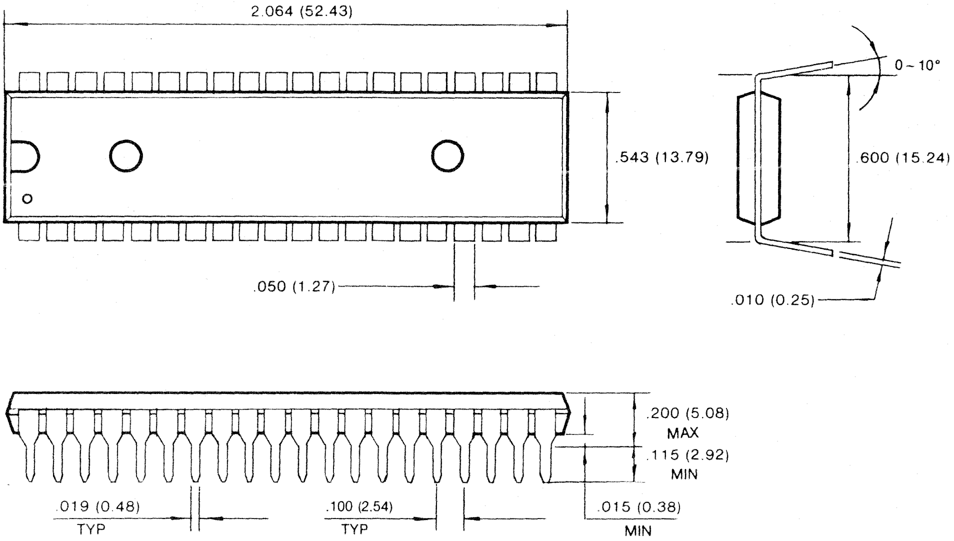
(*1) Byte Mode only. A-1 is Least Significant Bit Address. ($BHE = V_{IL}$)
(*2) Word Mode only. ($BHE = V_{IH}$)

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4200B)

Units: Inches (millimeters)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  - **Operating: 50mA (max.)**
  - **Standby : 50μA (max.)**
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  - **32-pin, 525 mil, plastic SOP**

GENERAL DESCRIPTION

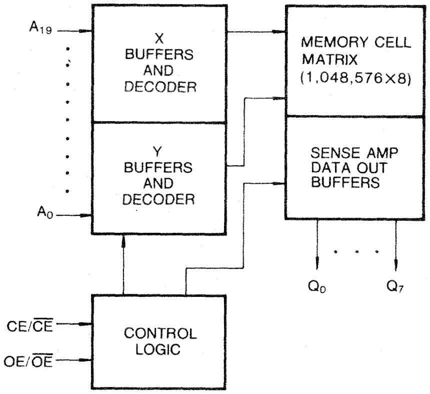
The KM23C8000A is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

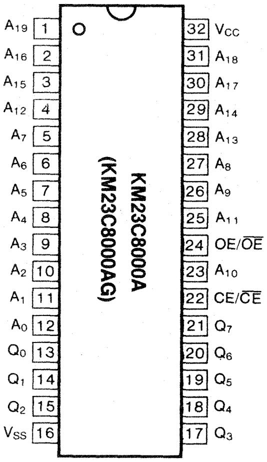
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8000A is packaged in a 32-DIP and the KM23C8000AG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	50	mA
	I_{CC2}		f=1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

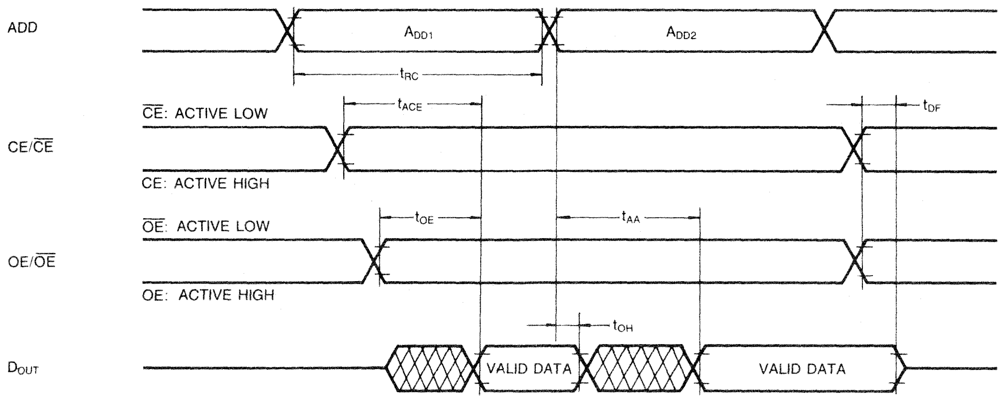
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8000A(G)-15		KM23C8000A(G)-20		KM23C8000A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

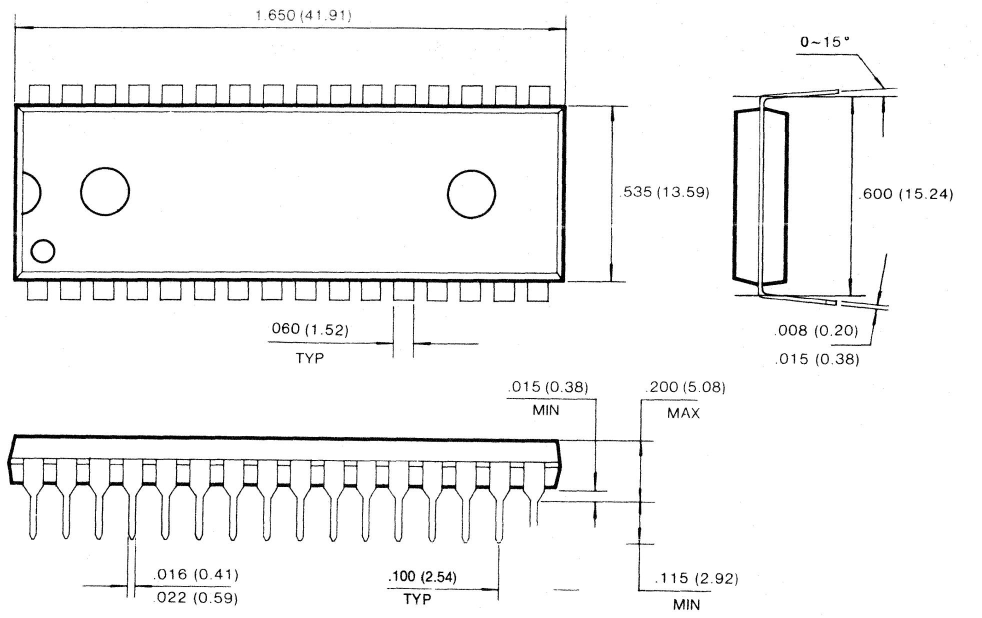


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

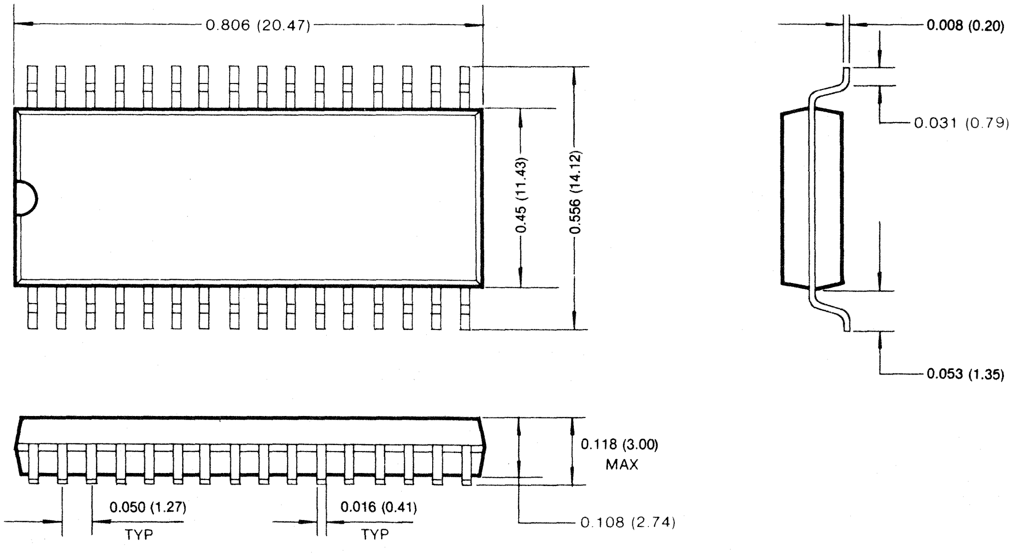
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8000AG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

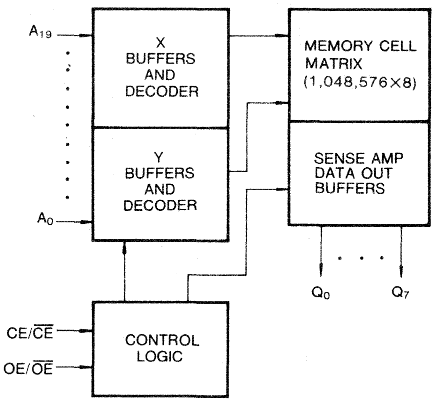
The KM23C8000H is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

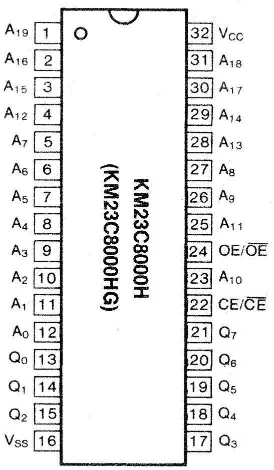
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8000H is packaged in a 32-DIP and the KM23C8000HG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

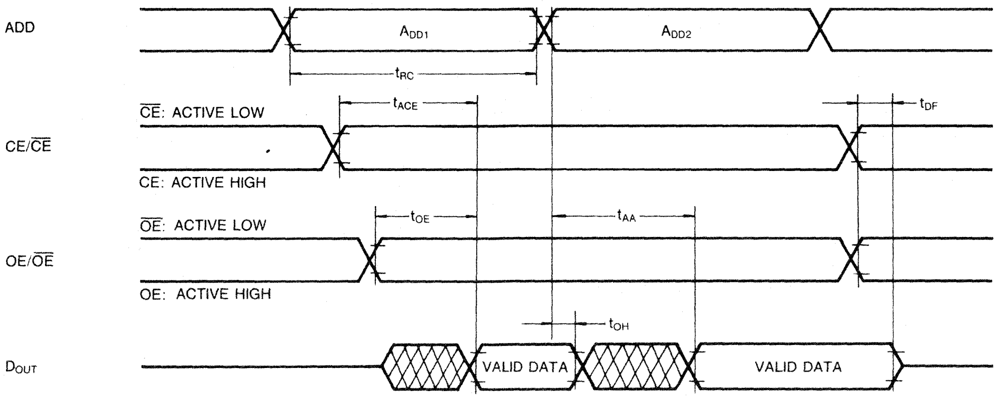
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8000H(G)-10		KM23C8000H(G)-12		KM23C8000H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

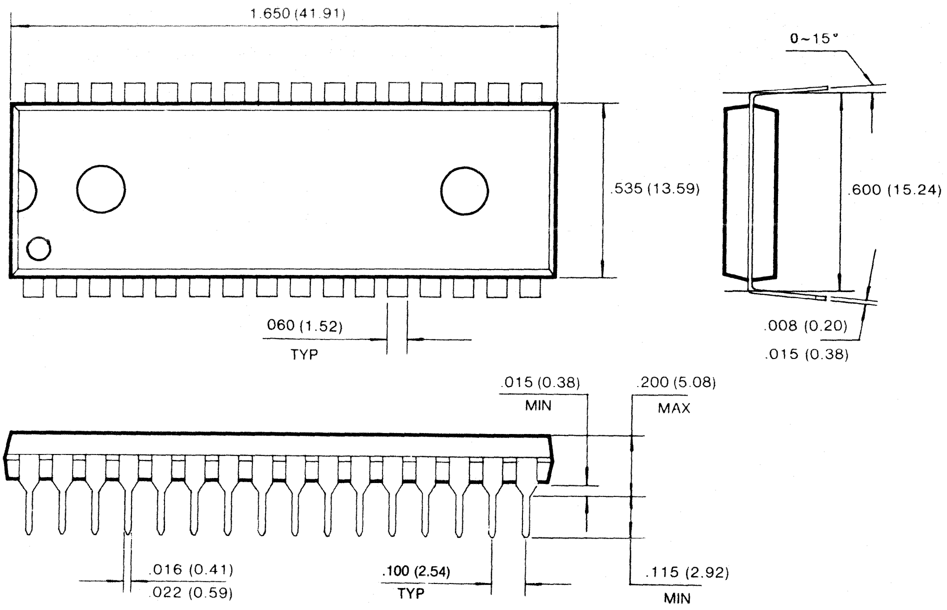


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

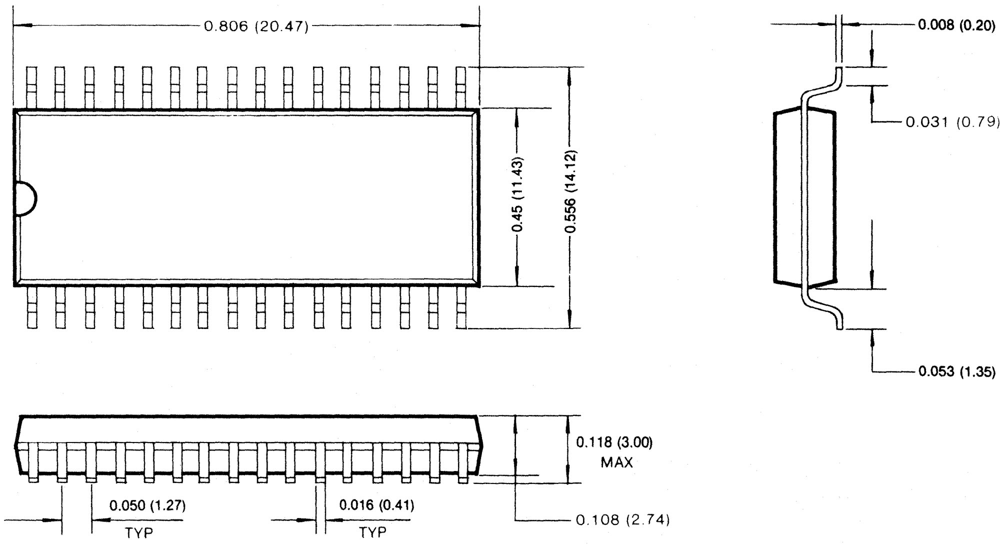
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8000HG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 × 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  - **Operating: 50mA (max.)**
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  - **32-pin, 525 mil, plastic SOP**

GENERAL DESCRIPTION

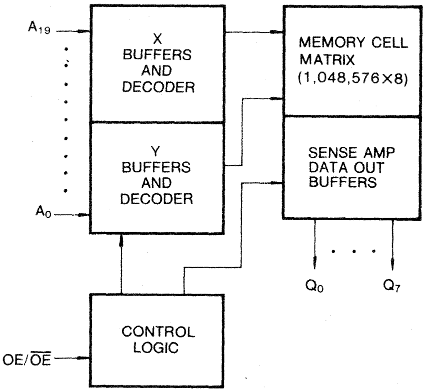
The KM23C8001A is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

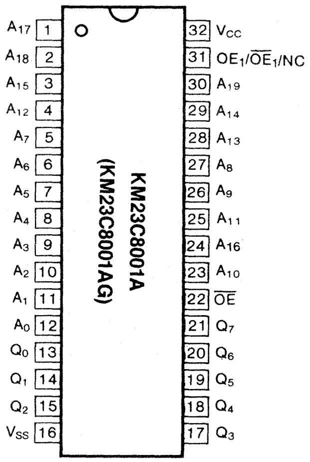
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8001A is packaged in a 32-DIP and the KM23C8001AG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	50	mA
	I_{CC2}		f=1.0MHz	—	25	mA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

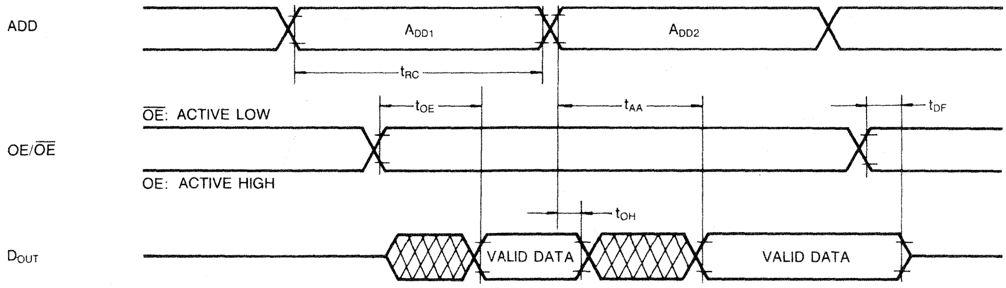
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8001A(G)-15		KM23C8001A(G)-20		KM23C8001A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

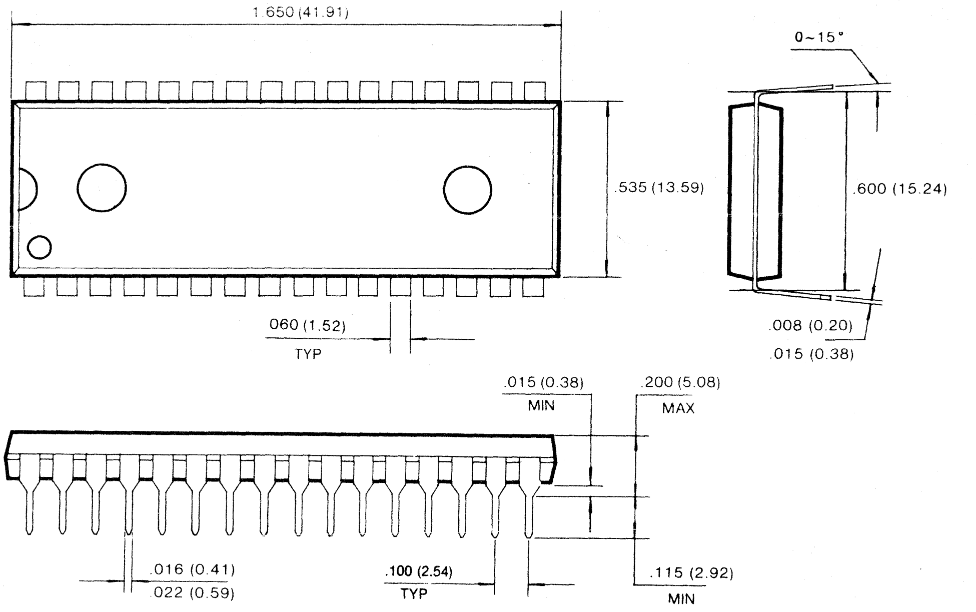
READ



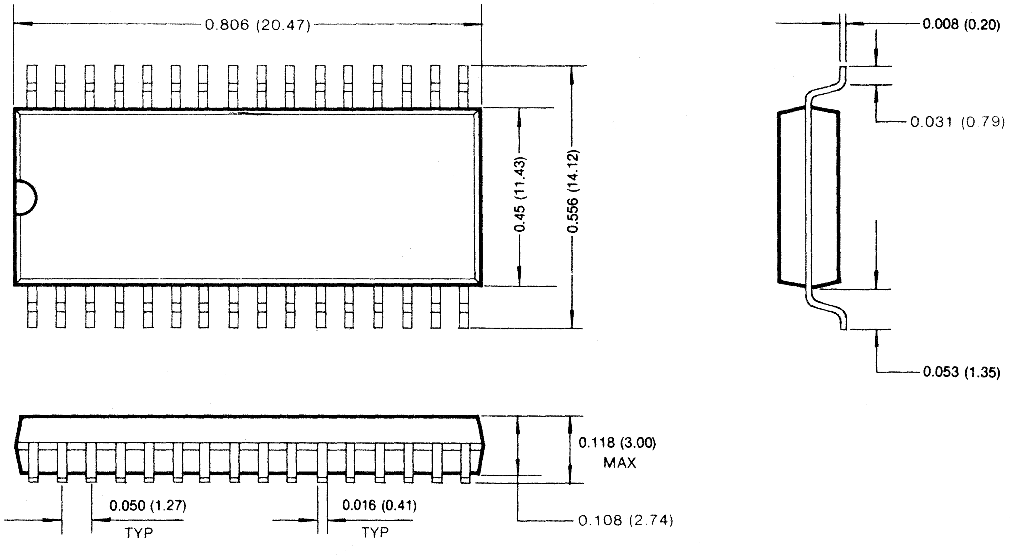
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8001A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8001AG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 × 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

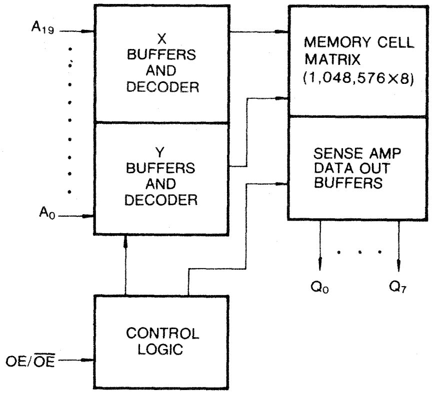
The KM23C8001H is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

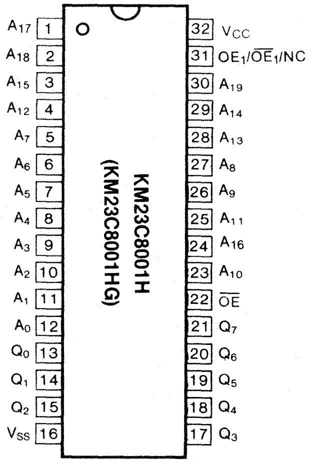
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8001H is packaged in a 32-DIP and the KM23C8001HG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

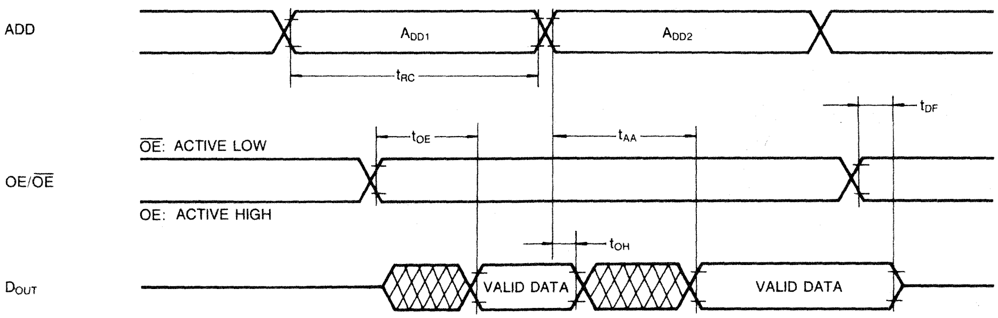
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8001H(G)-10		KM23C8001H(G)-12		KM23C8001H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

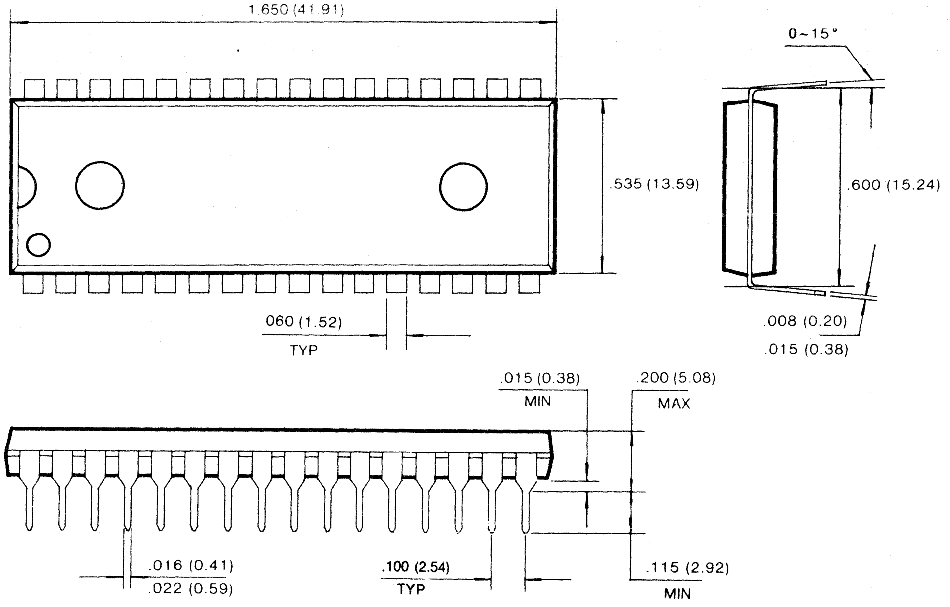
READ



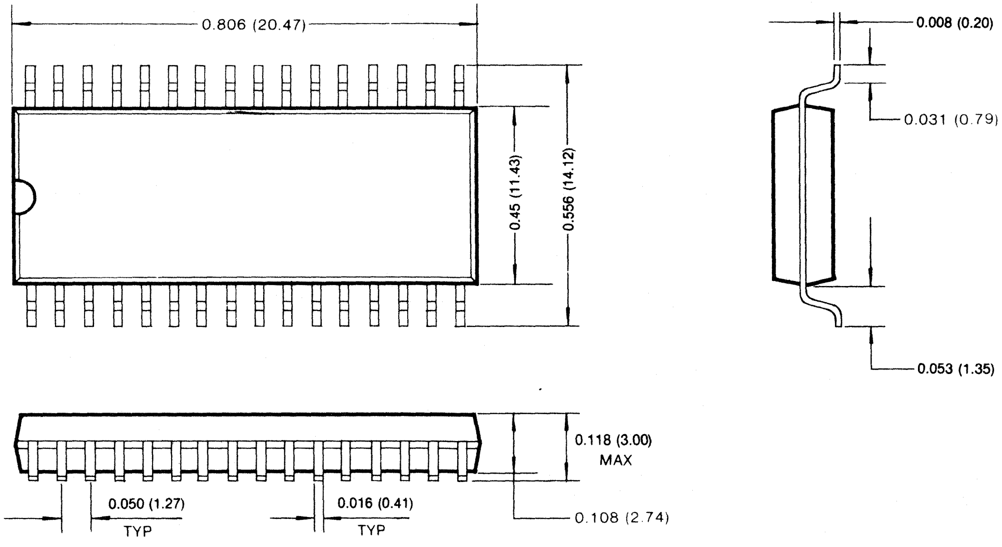
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8001H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8001HG)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  - **1,048,576 × 8 (byte mode)**
  - **524,288 × 16 (word mode)**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  - **Operating: 50mA (max.)**
  - **Standby : 50μA (max.)**
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)**
  - **44-pin, 600 mil, plastic SOP**

GENERAL DESCRIPTION

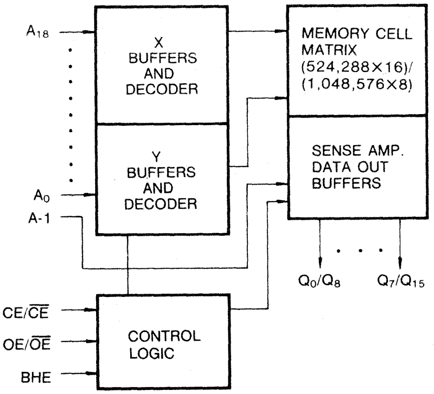
The KM23C8100A is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100A is packaged in a 42-DIP and the KM23C8100AG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

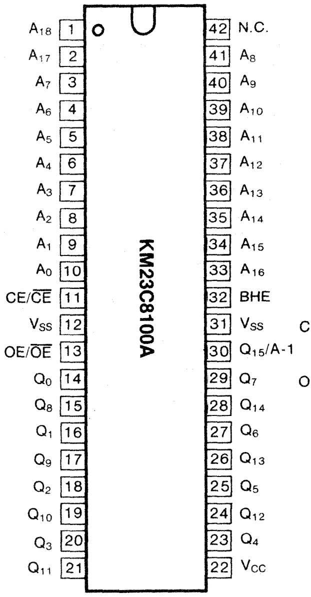
FUNCTIONAL BLOCK DIAGRAM

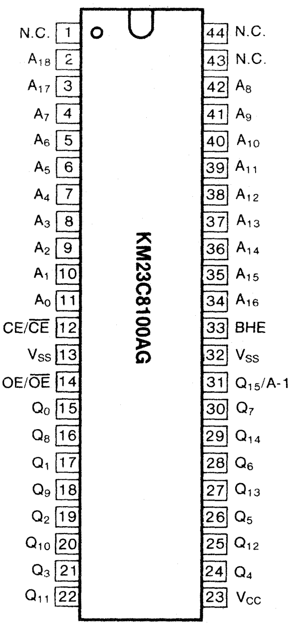


Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	50	mA
	I_{CC2}		f=1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE ($T_A=25$°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

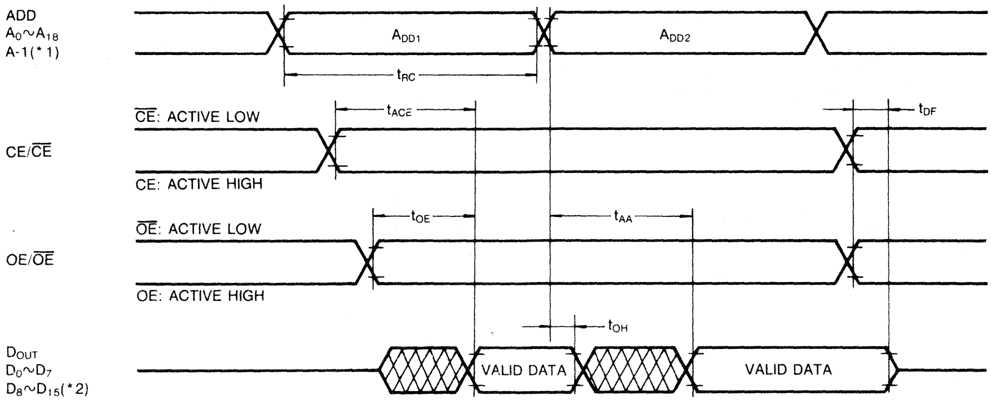
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100A(G)-15		KM23C8100A(G)-20		KM23C8100A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



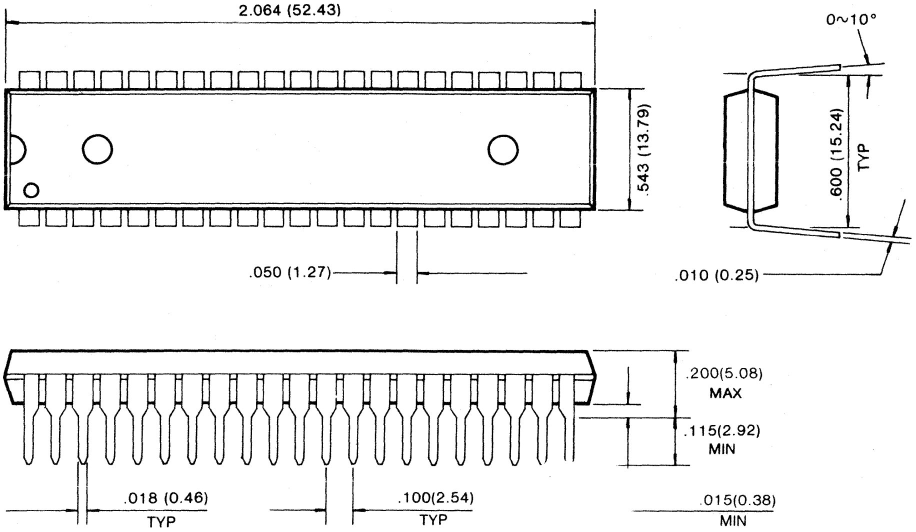
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

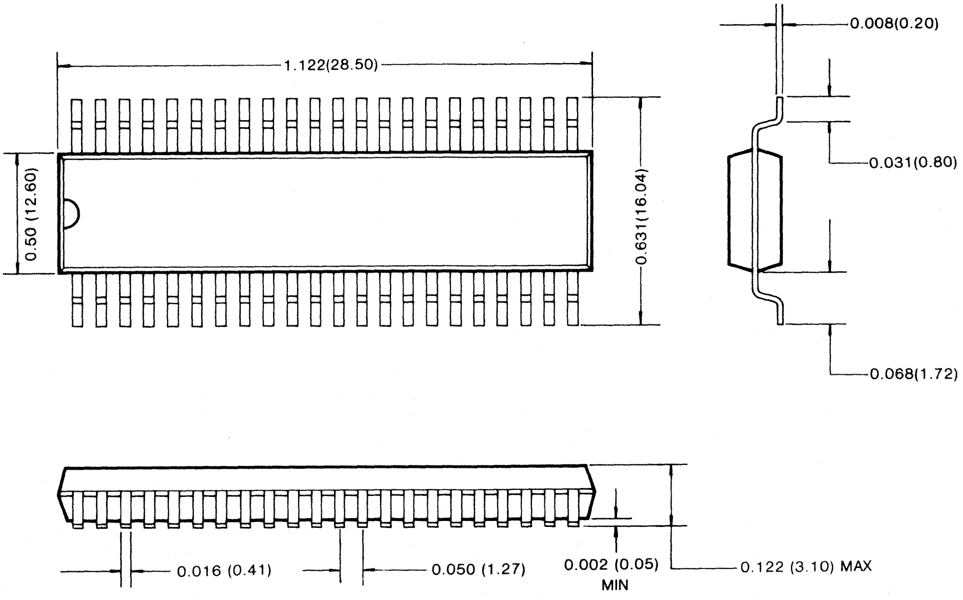
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8100A)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C8100AG)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 × 8 (byte mode)
  524,288 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

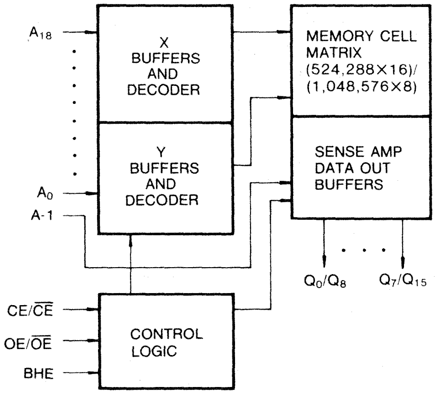
The KM23C8100AFP1 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576X8 bit (byte mode) or as 524,288X16 bit (word mode) depending on BHE (pin 29) voltage level. (See mode selection table)

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

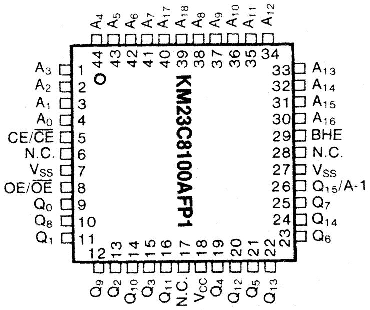
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100AFP1 is packaged in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A_{-1}	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

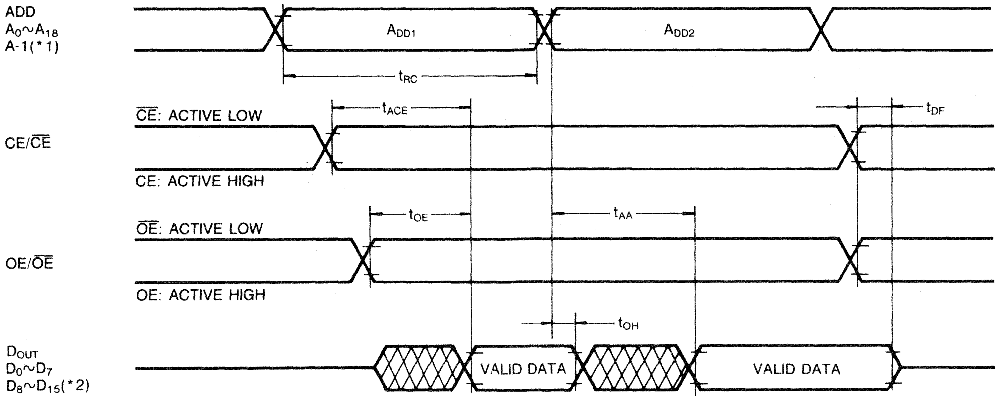
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100AFP1-15		KM23C8100AFP1-20		KM23C8100AFP1-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



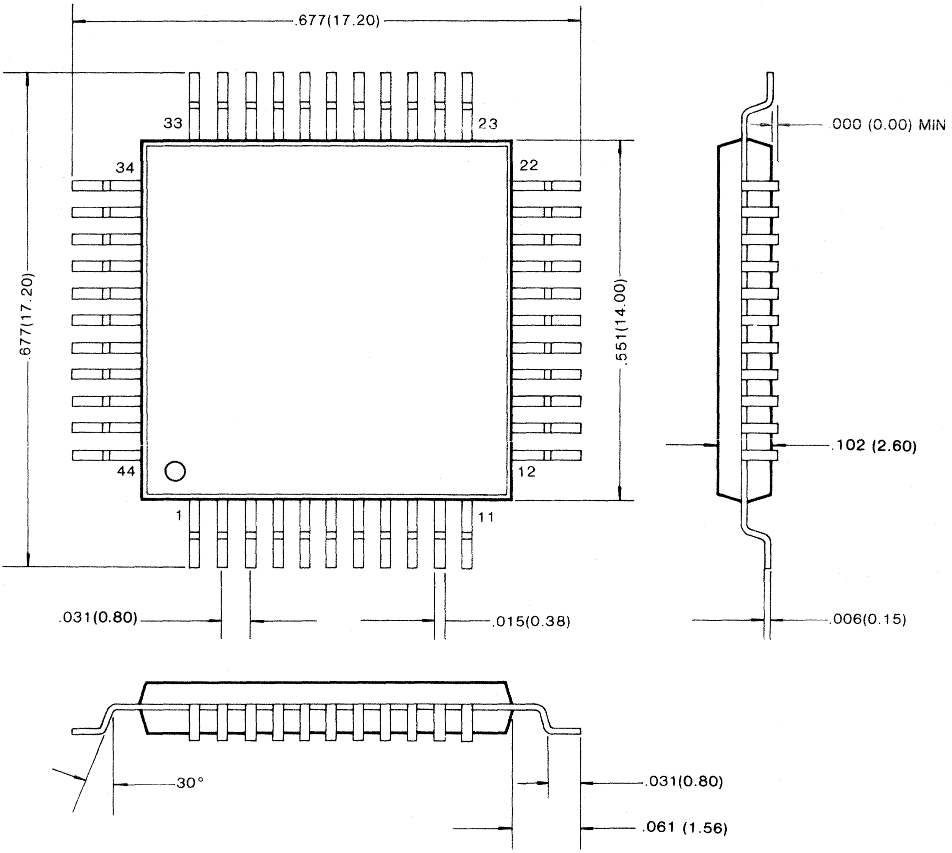
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

44 LEAD QUAD FLAT PACKAGE (KM23C8100AFP1)

Unit: Inches (mm)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 × 8 (byte mode)
  524,288 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

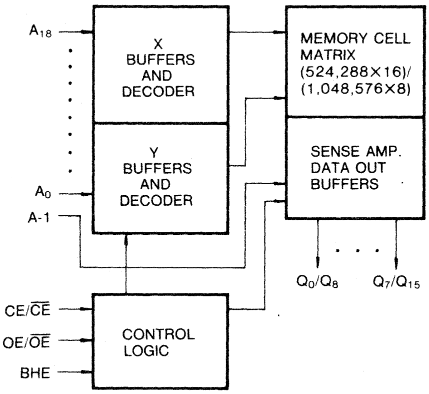
The KM23C8100AFP2 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE (pin 47) voltage level. (See mode selection table)

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

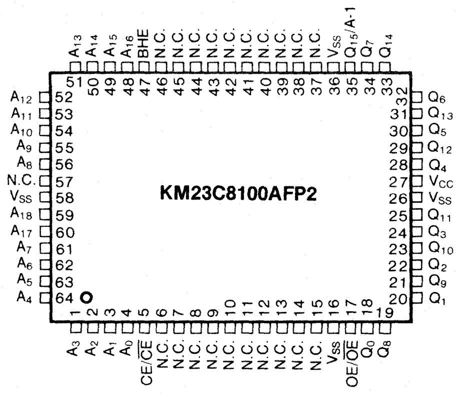
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100AFP2 is packaged in a 64-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Suppiy Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	50	mA
	I_{CC2}		f=1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

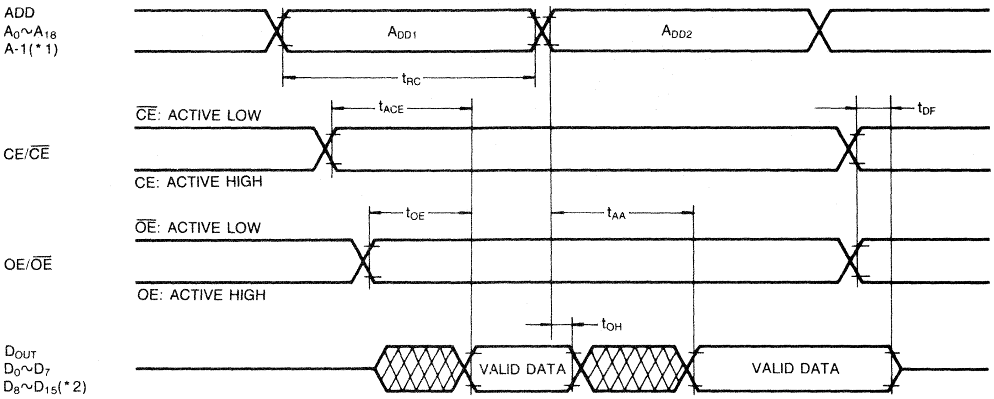
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100AFP2-15		KM23C8100AFP2-20		KM23C8100AFP2-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



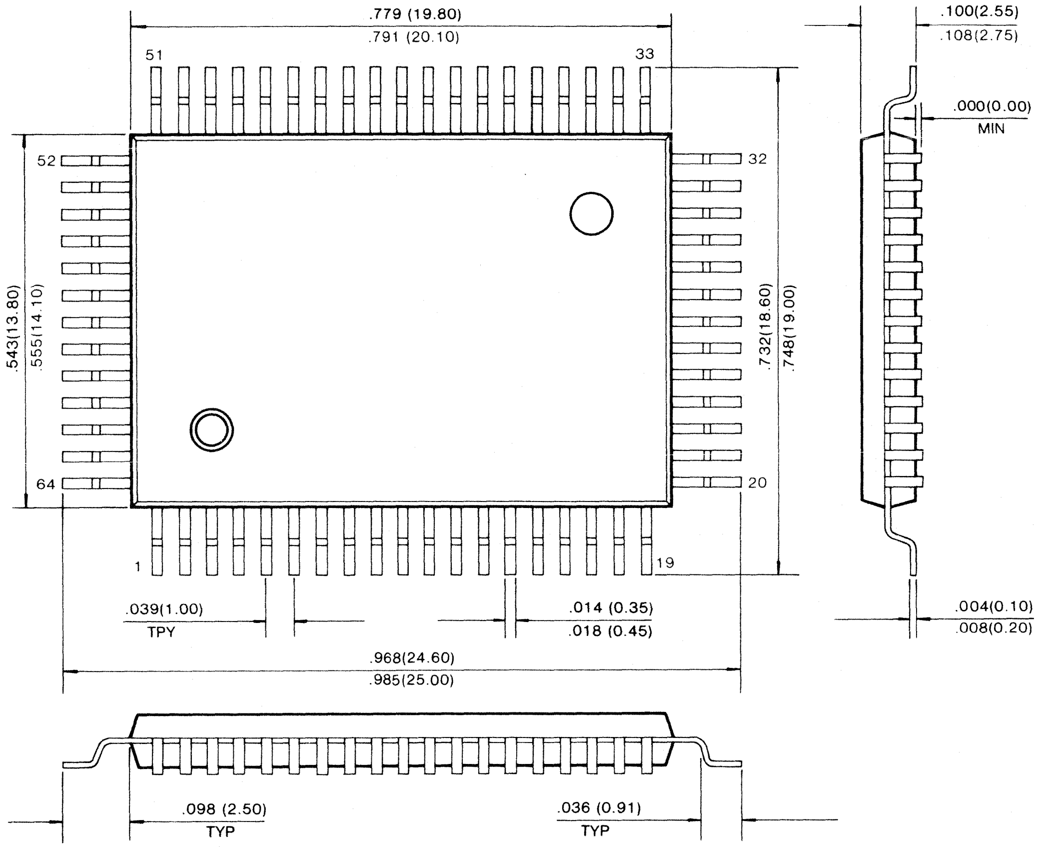
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

64 LEAD QUAD FLAT PACKAGE (KM23C8100AFP2)

Unit: Inches (mm)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 × 8 (byte mode)
  524,288 × 16 (word mode)
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)**
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

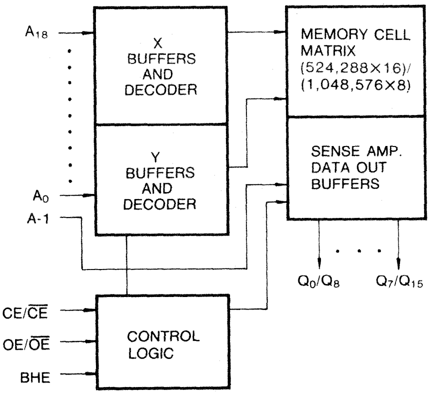
The KM23C8100H is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100H is packaged in a 42-DIP and the KM23C8100HG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

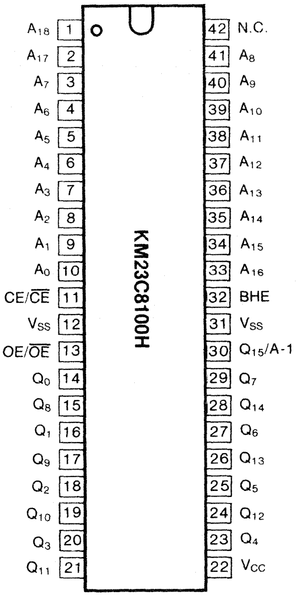
FUNCTIONAL BLOCK DIAGRAM

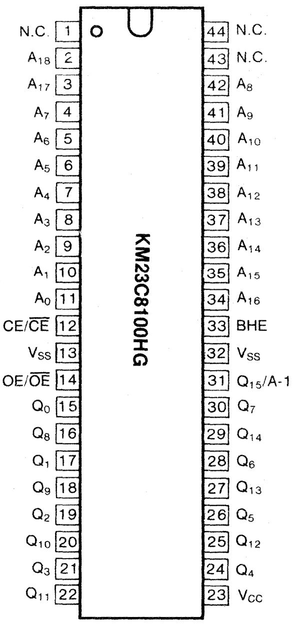


Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	60	mA
	I_{CC2}		f=1.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

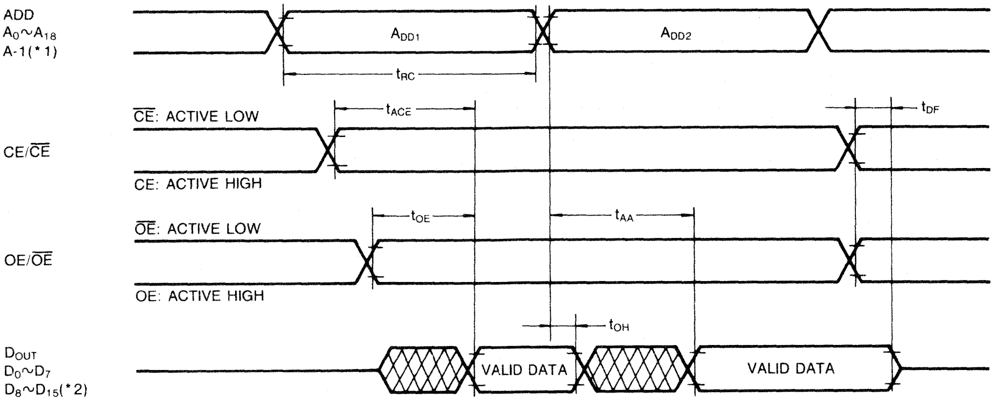
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100H(G)-10		KM23C8100H(G)-12		KM23C8100H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



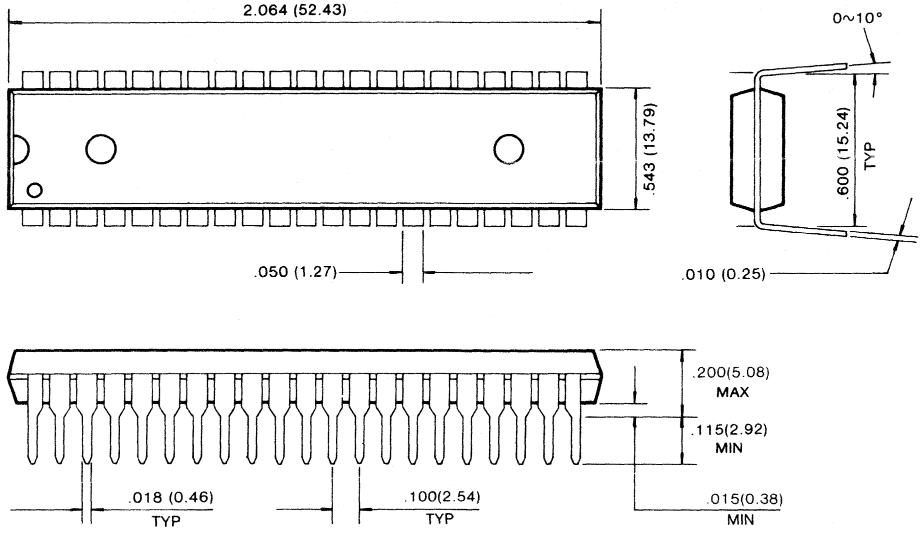
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

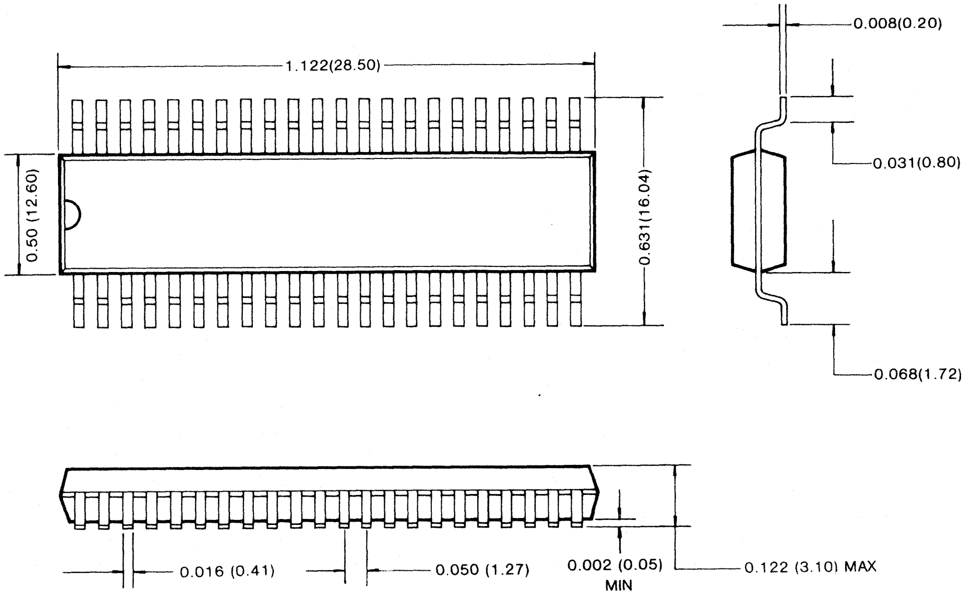
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8100H)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C8100HG)



KM23C8100HFP1

PRELIMINARY
CMOS MASK ROM

8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 × 8 (byte mode)
  524,288 × 16 (word mode)
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

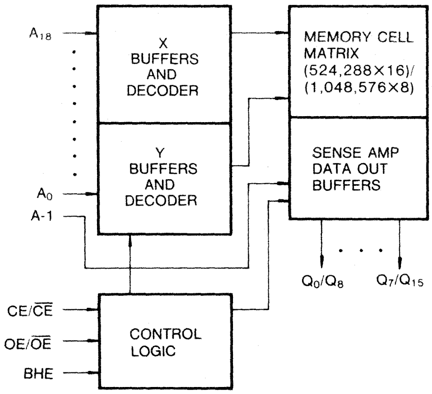
The KM23C8100HFP1 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE (pin 29) voltage level. (See mode selection table)

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

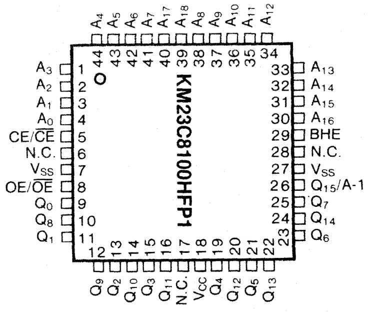
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100HFP1 is packaged in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	60	mA
	I_{CC2}		f=1.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

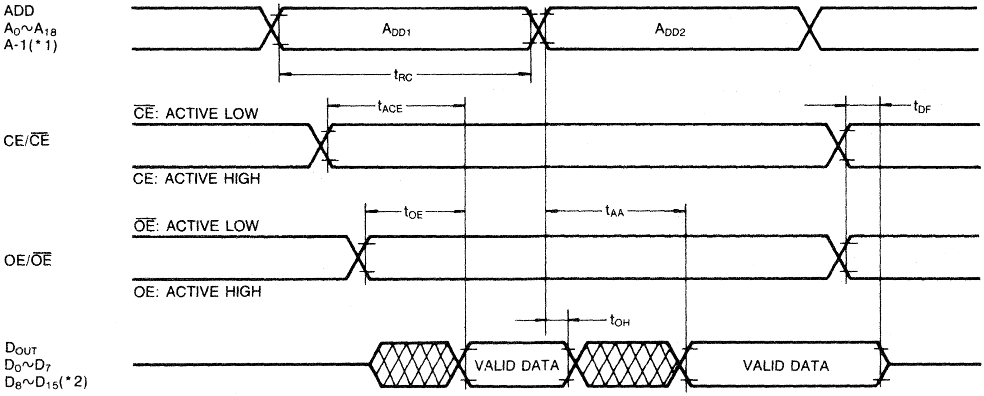
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100HFP1-10		KM23C8100HFP1-12		KM23C8100HFP1-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



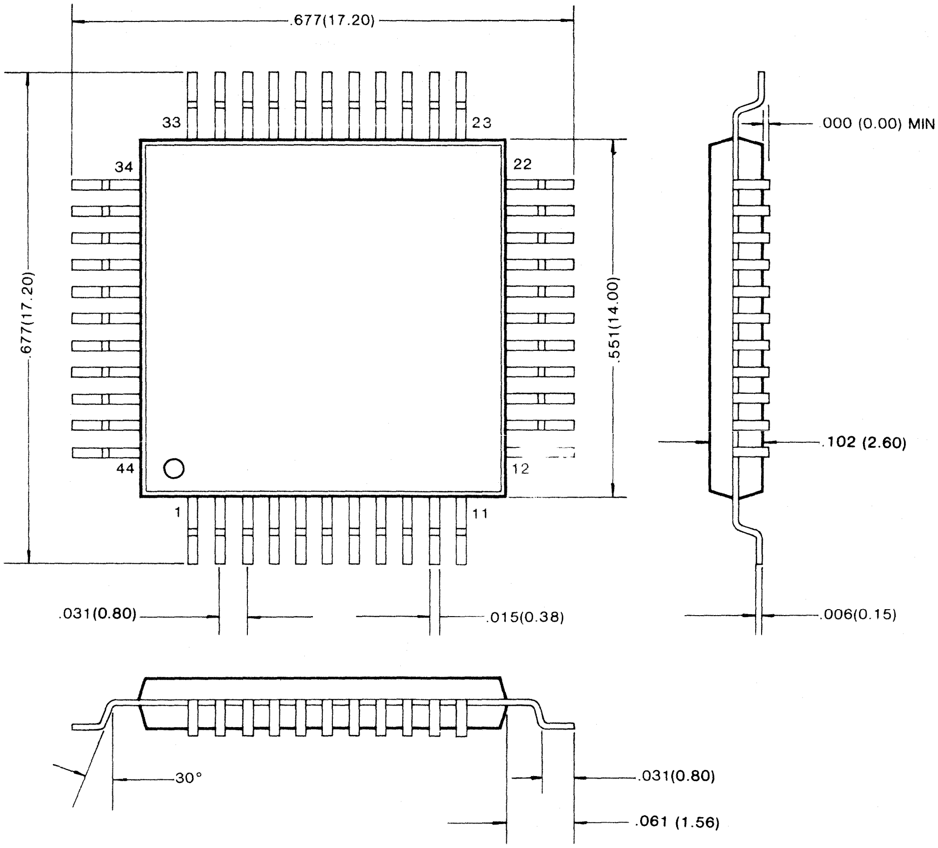
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

44 LEAD QUAD FLAT PACKAGE (KM23C8100HFP1)

Unit: Inches (mm)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 × 8 (byte mode)
  524,288 × 16 (word mode)
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

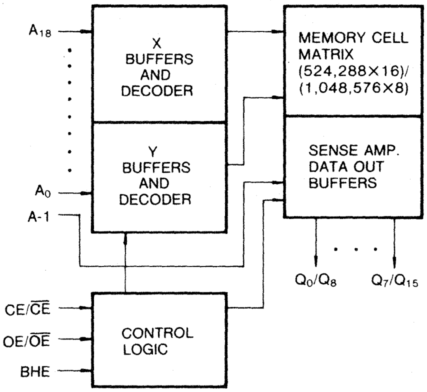
The KM23C8100HFP2 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE (pin 47) voltage level. (See mode selection table)

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

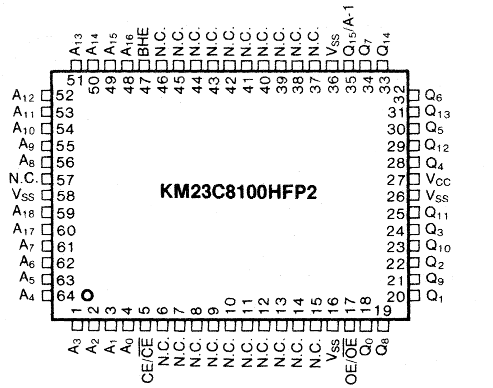
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100HFP2 is packaged in a 64-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	60	mA
	I_{CC2}		f = 1.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE ($T_A=25°C$, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

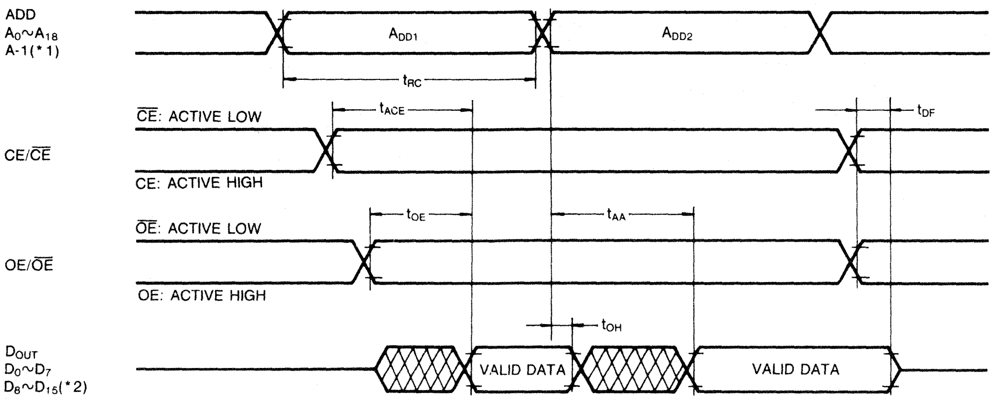
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C8100HFP2-10		KM23C8100HFP2-12		KM23C8100HFP2-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



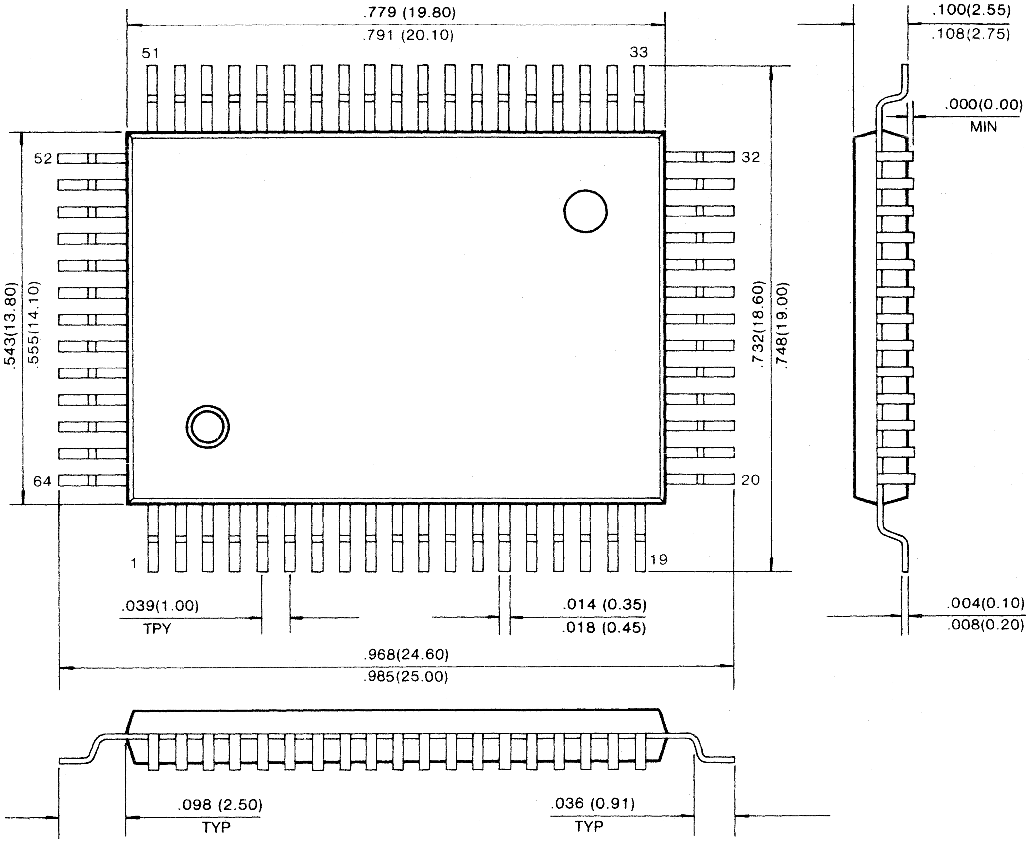
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

64 LEAD QUADFLAT PACKAGE (KM23C8100HFP2)

Unit: Inches (mm)



16M-Bit (2M X 8/1M X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 × 8 (byte mode)
  1,048,576 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)**
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

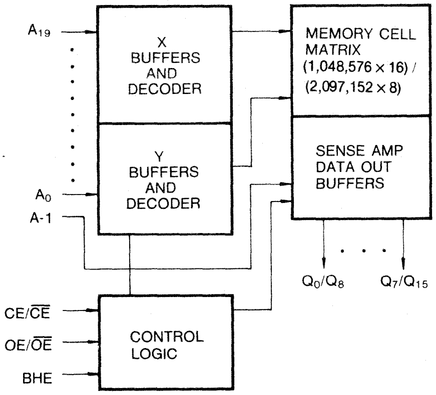
The KM23C16000 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organization either as 2,097,152X8 bit (byte mode) or as 1,048,576X16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16000 is packaged in a 42-DIP, and the KM23C16000G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

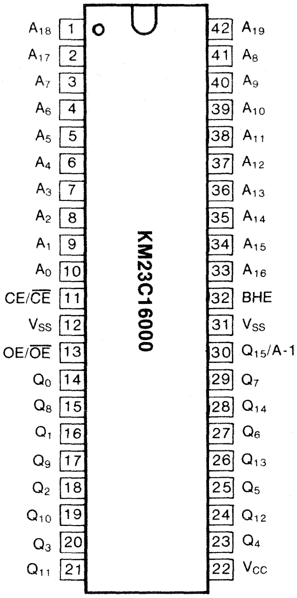
FUNCTIONAL BLOCK DIAGRAM

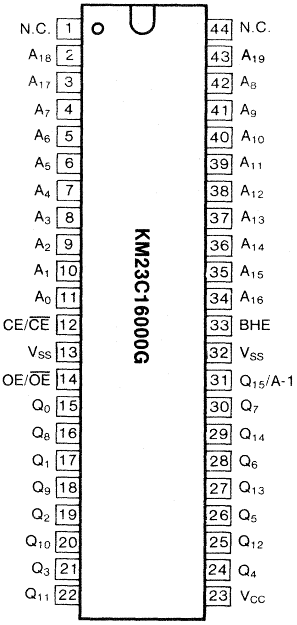


Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{\text{CE}}$*	Chip Enable
OE/$\overline{\text{OE}}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f=6.7MHz	—	50	mA
	I_{CC2}		f=1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

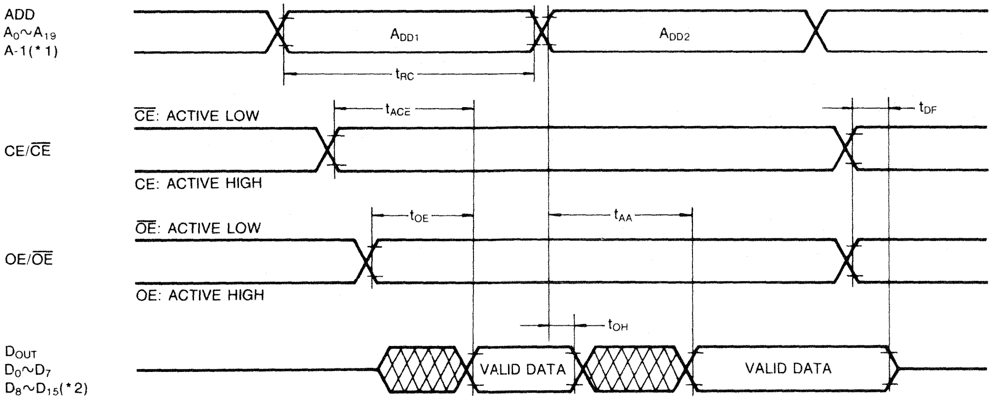
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C16000(G)-15		KM23C16000(G)-20		KM23C16000(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



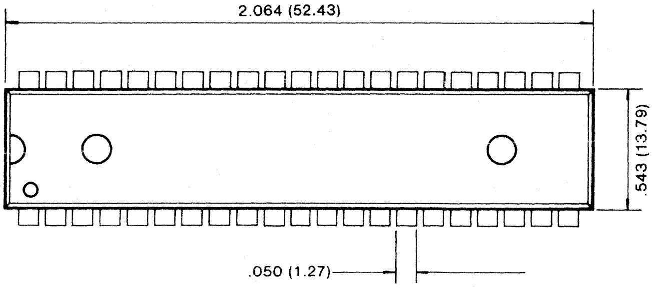
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

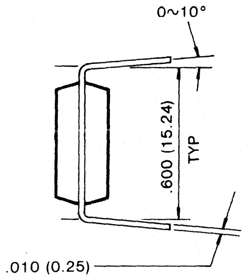
* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

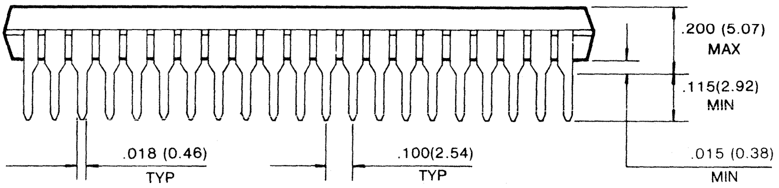
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16000)

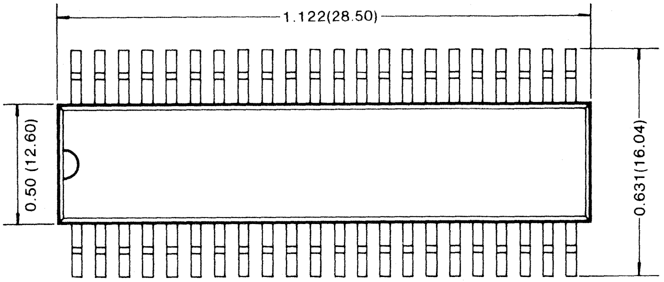
Unit: Inches (mm)

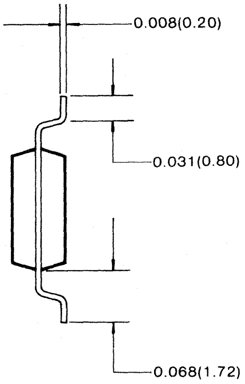


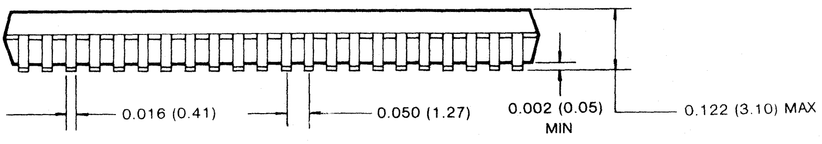




44 LEAD SMALL OUTLINE PACKAGE (KM23C16000G)







16M-Bit (2MX8/1MX16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 × 8 (byte mode)
  1,048,576 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

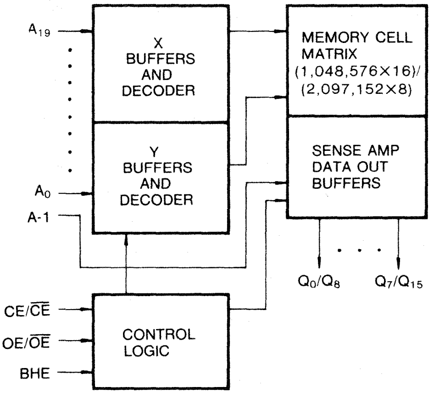
The KM23C16000FP is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152X8 bit (byte mode) or as 1,048,576X16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

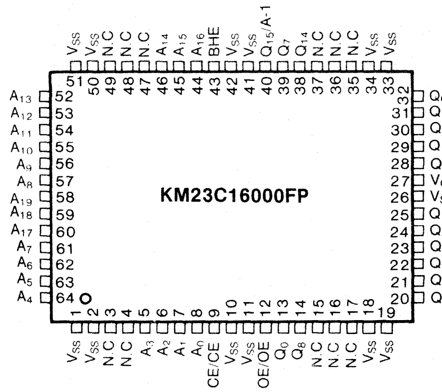
It is suitable for use in program memory of micorprocessr, and data memory, character generator.

The KM23C16000FP is packaged in a 64-QFP provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	50	mA
	I_{CC2}		f = 1.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

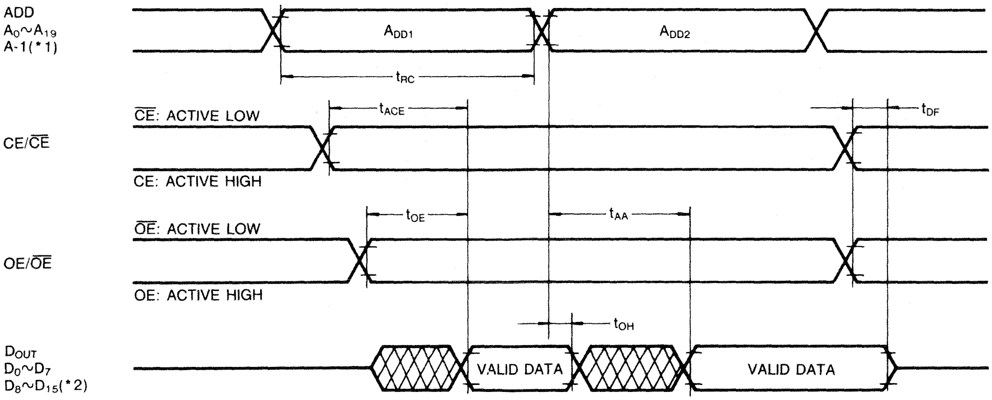
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C16000FP-15		KM23C16000FP-20		KM23C16000FP-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



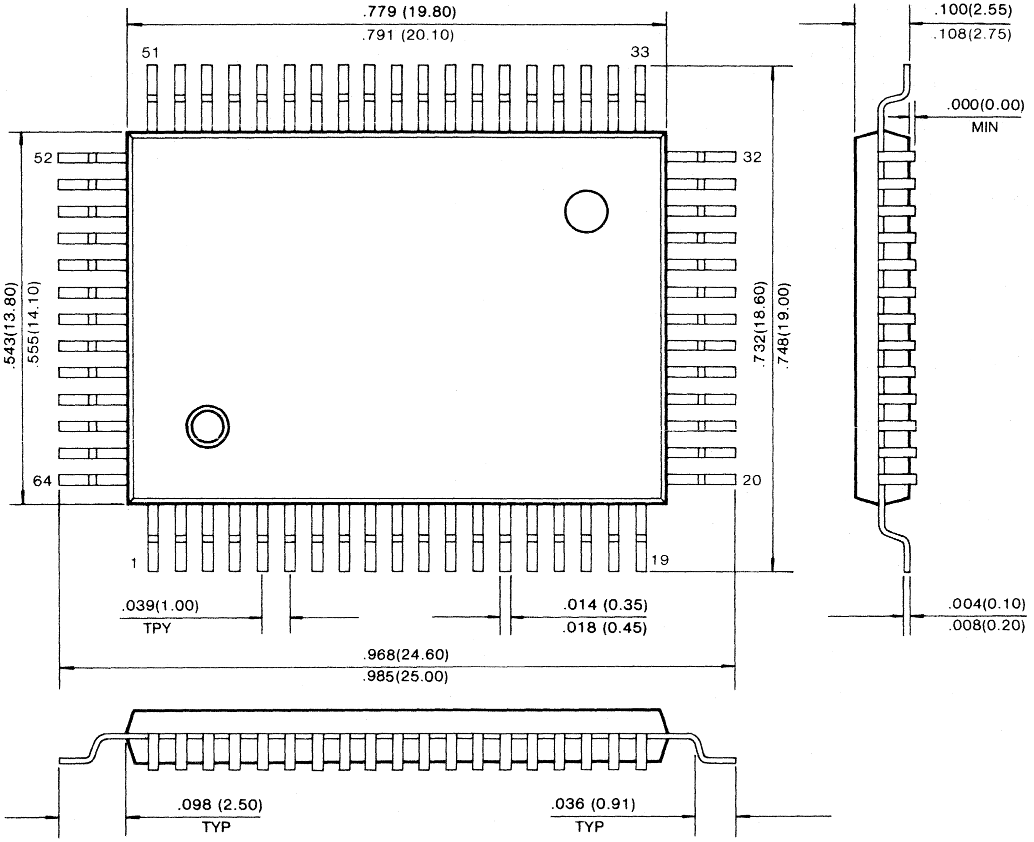
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

64 LEAD QUADFLAT PACKAGE (KM23C16000FP)

Unit: Inches (mm)



PRELIMINARY

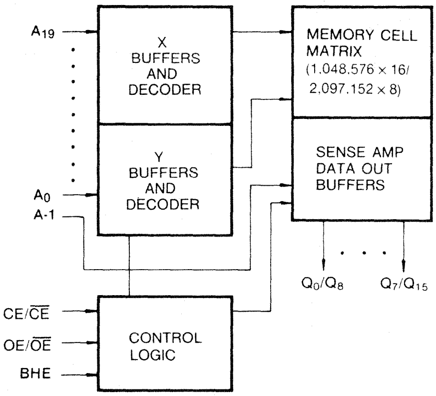
KM23C16100 CMOS MASK ROM

16M-Bit (2M × 8/1M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 × 8 (byte mode)
  1,048,576 × 16 (word mode)
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

GENERAL DESCRIPTION

The KM23C16100 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152 × 8 bit (byte mode) or as 1,048,576 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table)

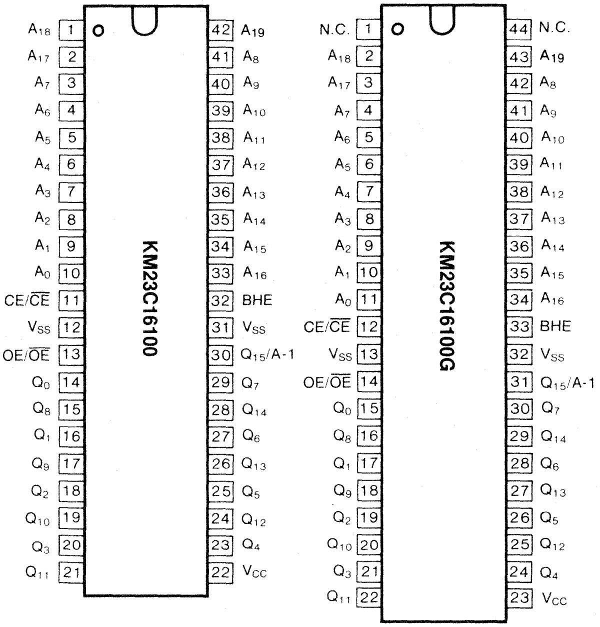
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{19} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16100 is packaged in a 42-DIP and the KM23C16100G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	$f = 6.7MHz$	—	100	mA
	I_{CC2}		$f = 1.0MHz$	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25°C$, $f = 1.0MHz$)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

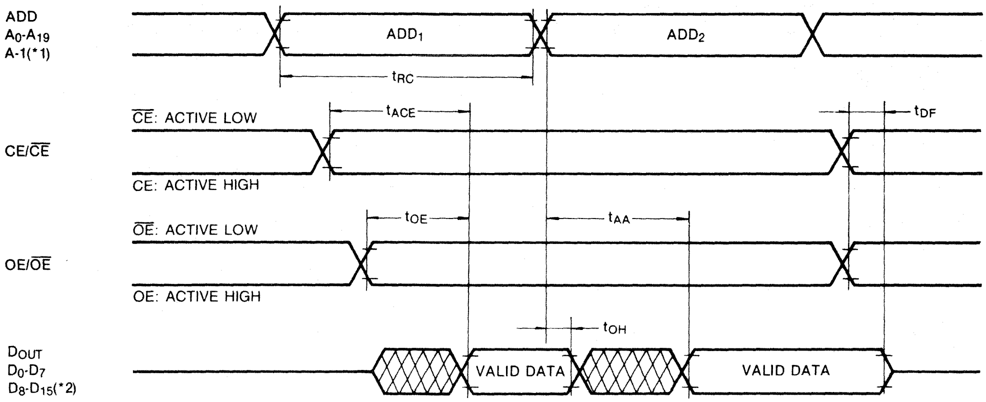
READ CYCLE

Parameter	Symbol	KM23C16100(G)-15		KM23C16100(G)-20		KM23C16100(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

* Page Address: A_0, A_1, A_2

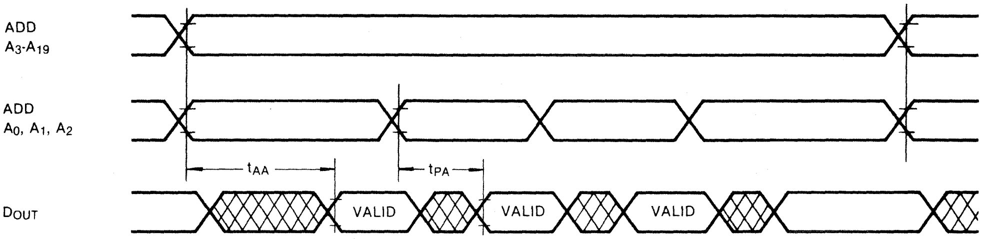
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

PAGE READ

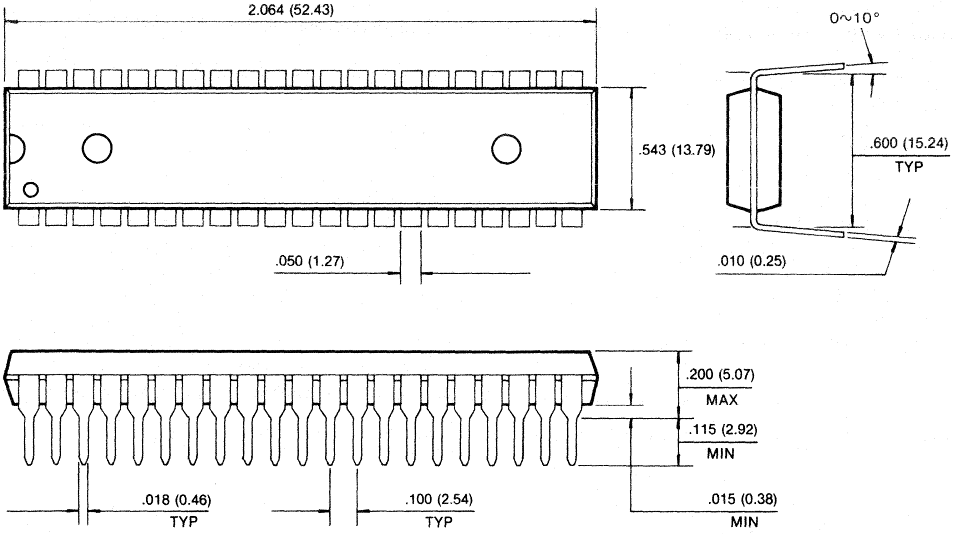


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

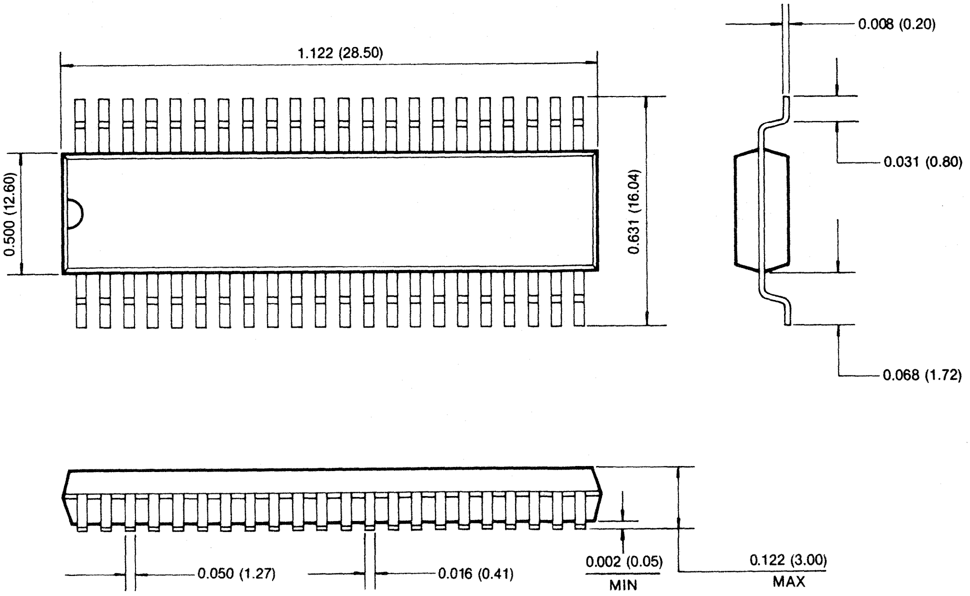
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16100)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C16100G)



16M-Bit (2MX8/1MX16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 × 8 (byte mode)
  1,048,576 × 16 (word mode)
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

The KM23C16100FP is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152 × 8 bit (byte mode) or as 1,048,576 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table)

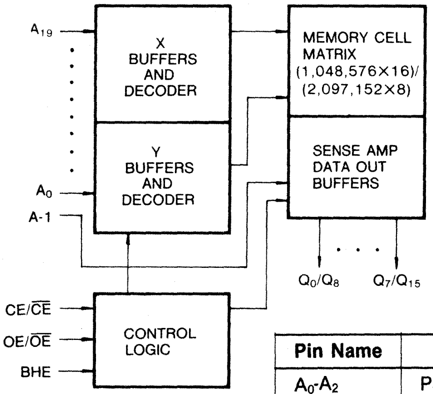
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{19} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

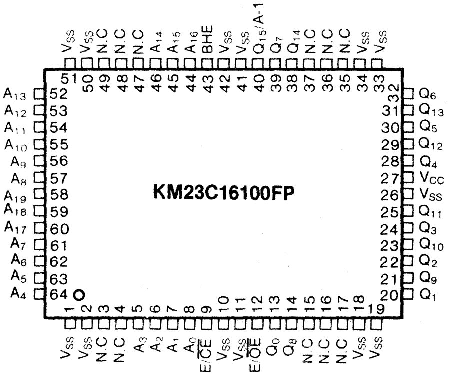
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16100FP is packaged in a 64-QFP provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	100	mA
	I_{CC2}		f = 1.0MHz	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25$°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

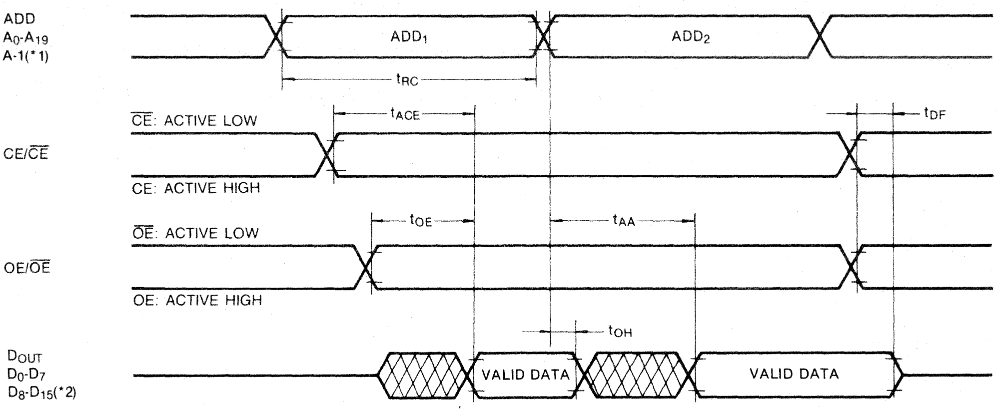
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C16100FP-15		KM23C16100FP-20		KM23C16100FP-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

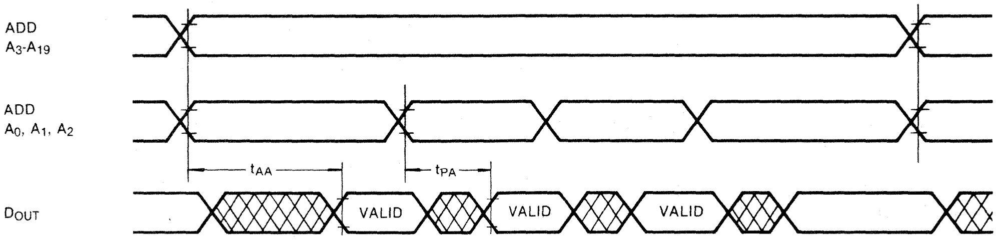
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

PAGE READ

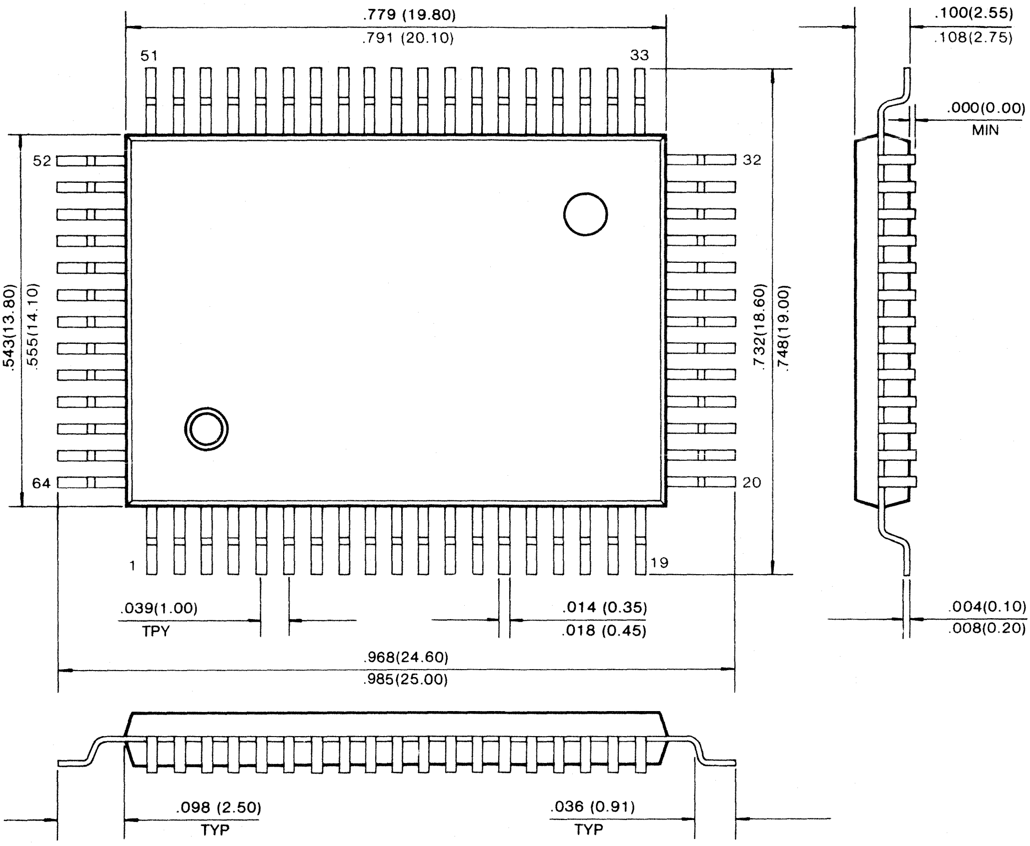


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

64 LEAD QUADFLAT PACKAGE (KM23C16100FP)

Unit: Inches (mm)



32M-Bit (2M × 16) CMOS MASK ROM

FEATURES

- **2,097,152 × 16 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)**

GENERAL DESCRIPTION

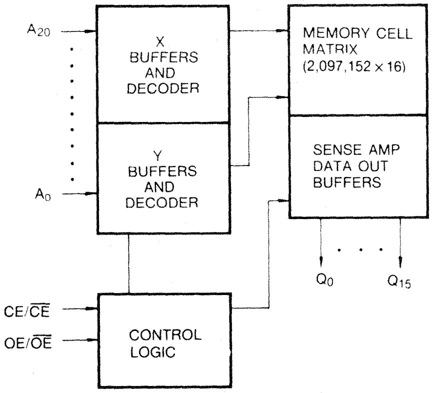
The KM23C32000 is a fully static mask programmable ROM organized 2,097,152 × 16 bit. It is fabricated using silicon gate CMOS process technolgy.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C32000 is packaged in a 42-DIP provides polarity programmable CE and OE buffer as user option mode.

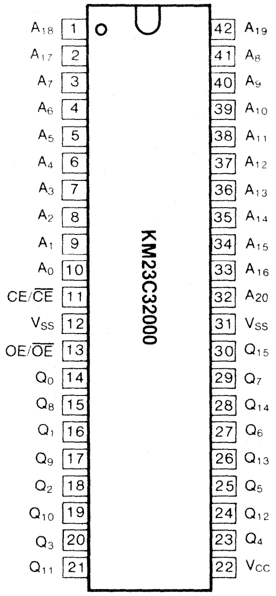
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_{15}	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	60	mA
	I_{CC2}		f = 1.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

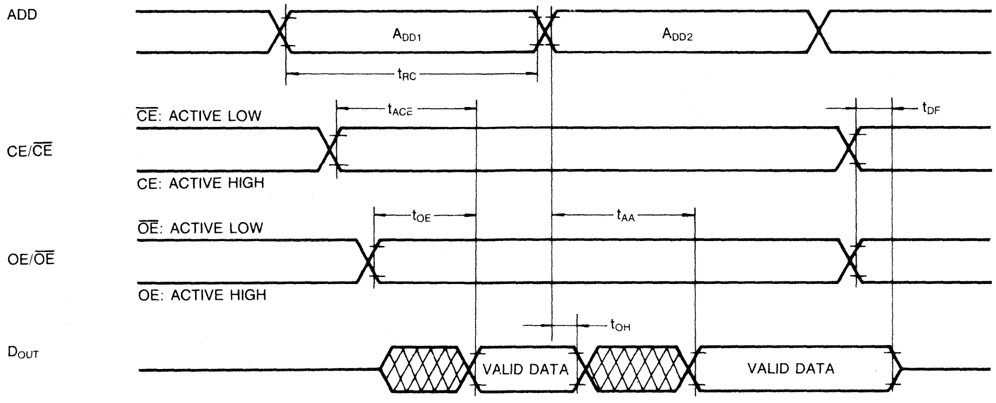
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C32000-15		KM23C32000-20		KM23C32000-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

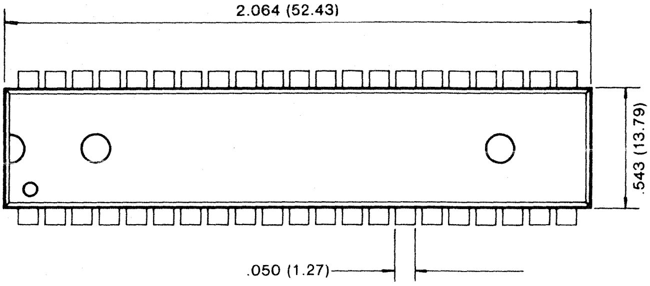


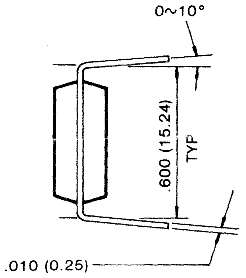
* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

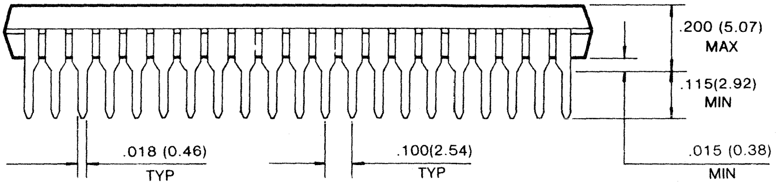
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C32000)

Unit: Inches (mm)







32M-Bit (4M × 8/2M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 × 8 (byte mode)
  2,097,152 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin, 600 mil, plastic SOP**

GENERAL DESCRIPTION

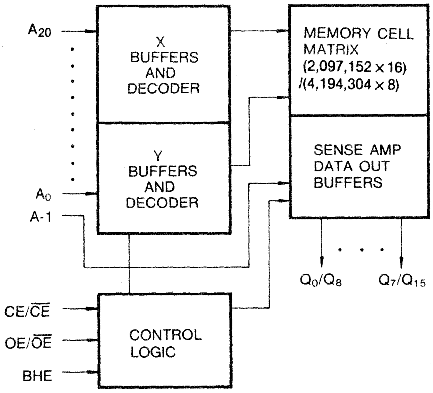
The KM23C32000G is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organization either as 4,194,304 × 8 bit (byte mode) or as 2,097,152 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32000G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

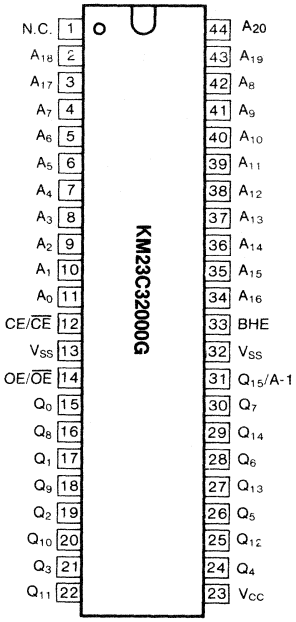
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	60	mA
	I_{CC2}		f = 1.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

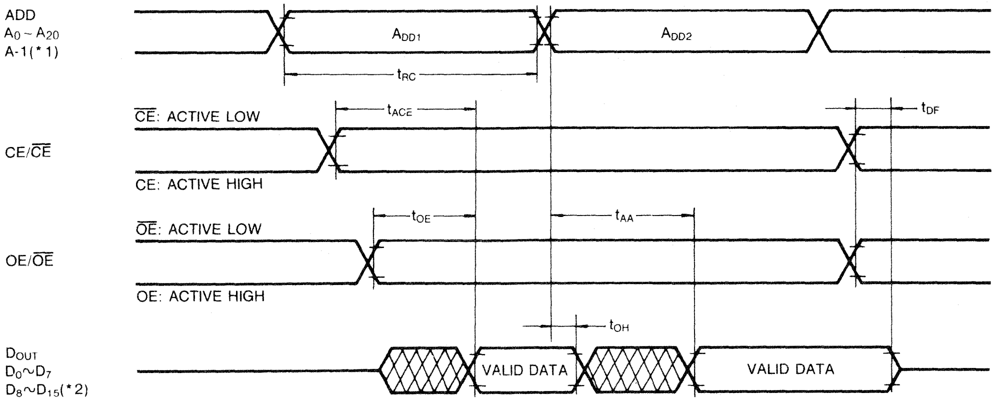
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C32000G-15		KM23C32000G-20		KM23C32000G-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ

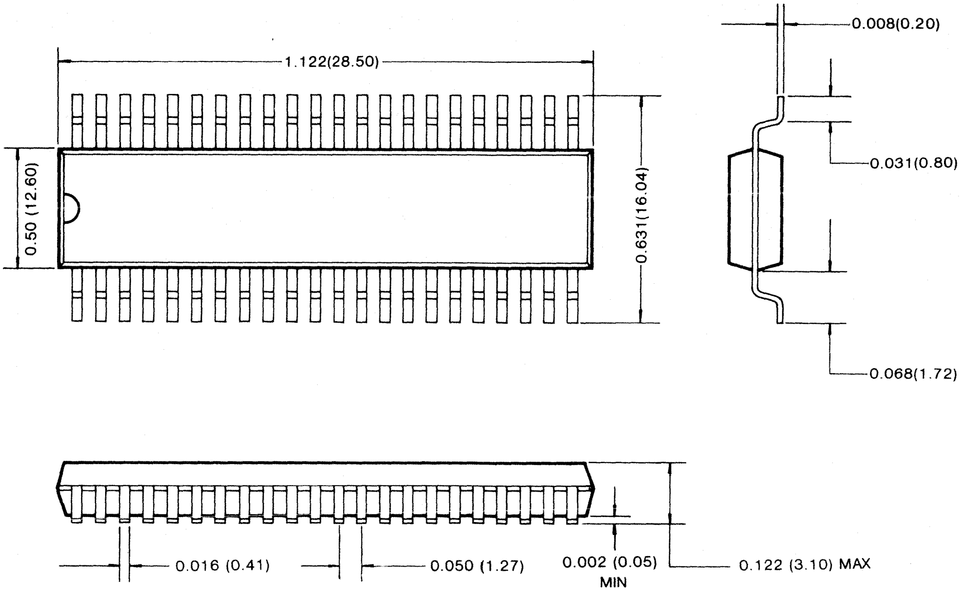


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

44 LEAD SMALL OUTLINE PACKAGE (KM23C32000G)

Unit: Inches (mm)



32M-Bit (4M × 8/2M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 × 8 (byte mode)
  2,097,152 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

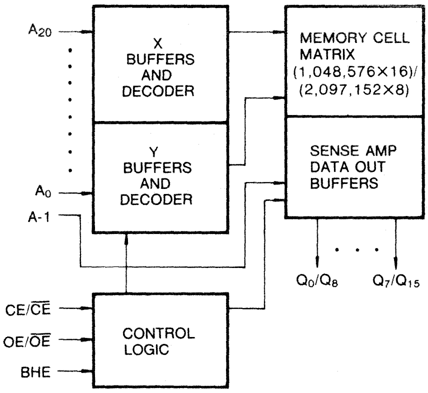
The KM23C32000FP is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 × 8 bit (byte mode) or as 2,097,152 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

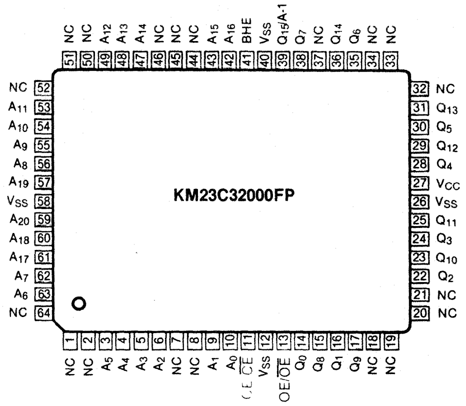
It is suitable for use in program memory of micorprocessr, and data memory, character generator.

The KM23C32000FP is packaged in a 64-QFP provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, [illegible] 7MHz all output ope [illegible]	—	60	mA
	I_{CC2}	[illegible] MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$	—	0.4	V

CAPACITANCE (T_a=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

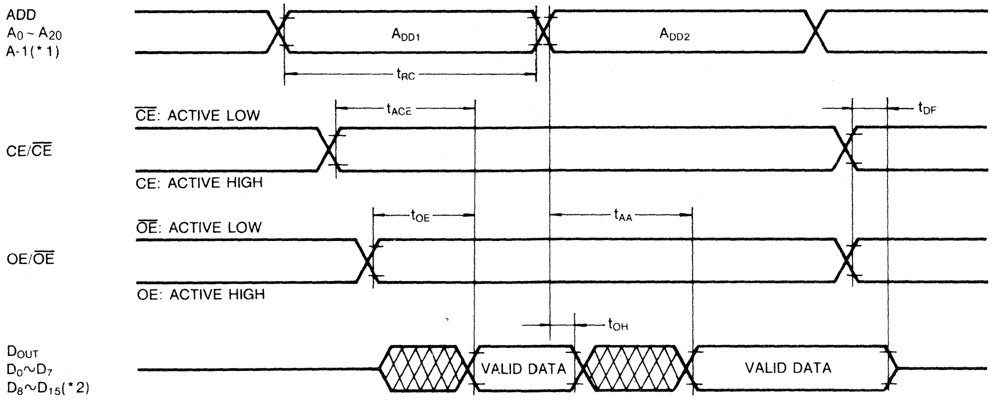
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C32000FP-15		KM23C32000FP-20		KM23C32000FP-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



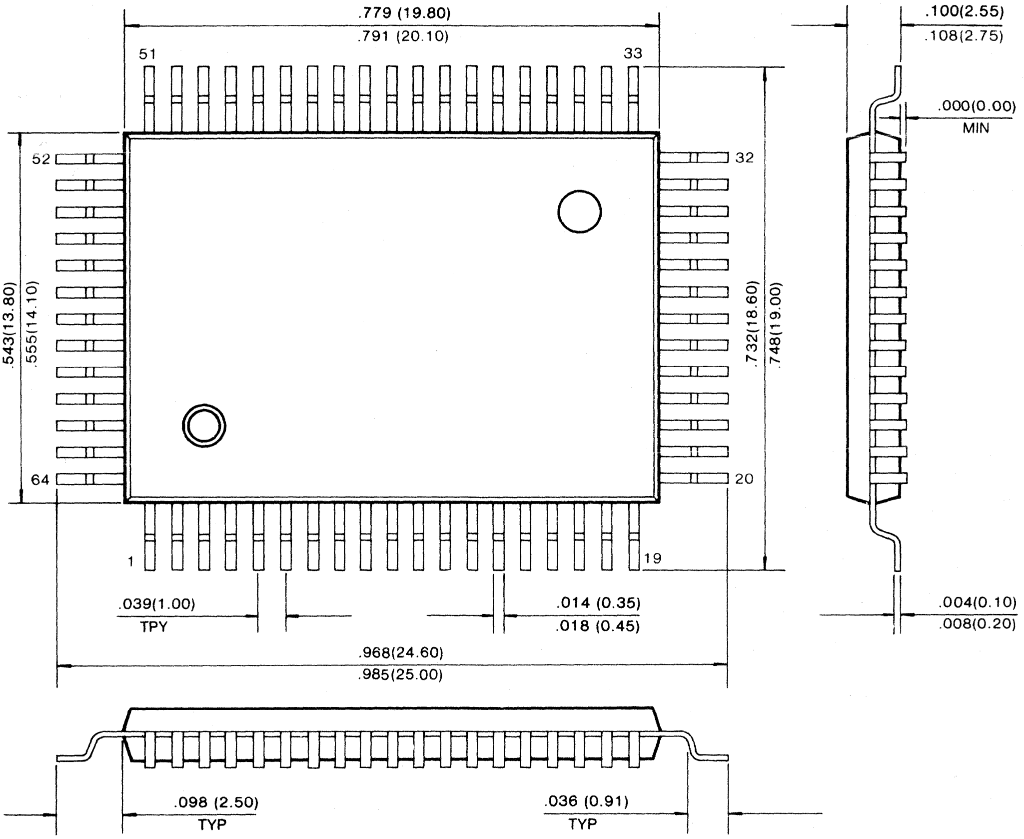
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

64 LEAD QUADFLAT PACKAGE (KM23C32000FP)

Unit: Inches (mm)



32M-Bit (2M × 16) CMOS MASK ROM

FEATURES

- **2,097,152 × 16 bit organization**
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)

GENERAL DESCRIPTION

The KM23C32100 is a fully static mask programmable ROM organized 2,097,152 × 16 bit. It is fabricated using silicon gate CMOS process technology.

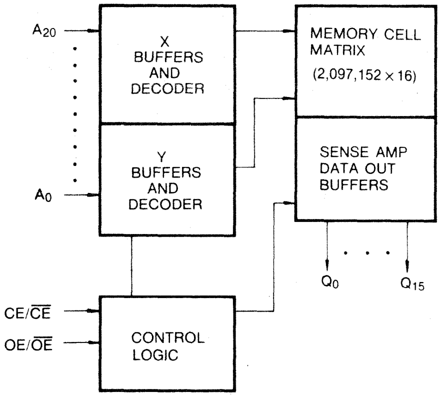
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{20} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C32100 is packaged in a 42-DIP provides polarity programmable CE and OE buffer as user option mode.

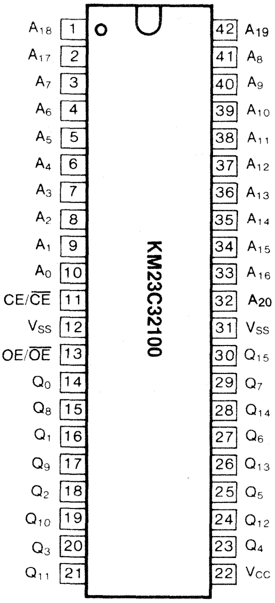
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{20}	Address Inputs
Q_0-Q_{15}	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	$f = 6.7MHz$	—	100	mA
	I_{CC2}		$f = 1.0MHz$	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25$°C, $f = 1.0MHz$)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

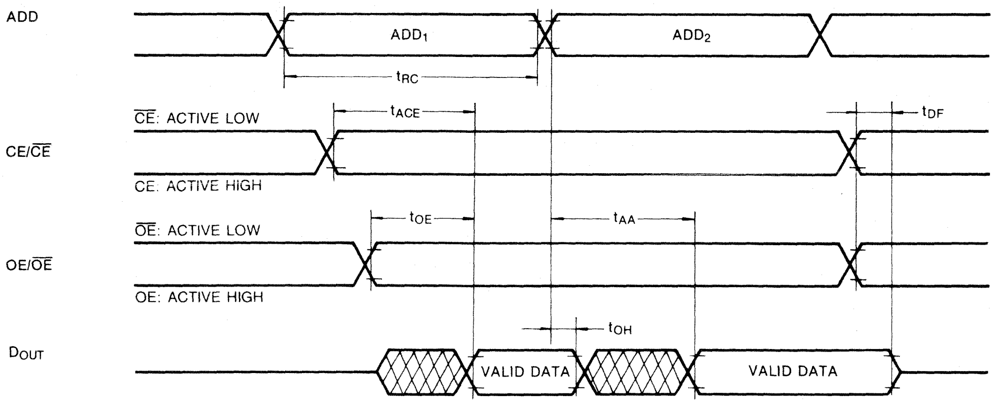
READ CYCLE

Parameter	Symbol	KM23C32100-15		KM23C32100-20		KM23C32100-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

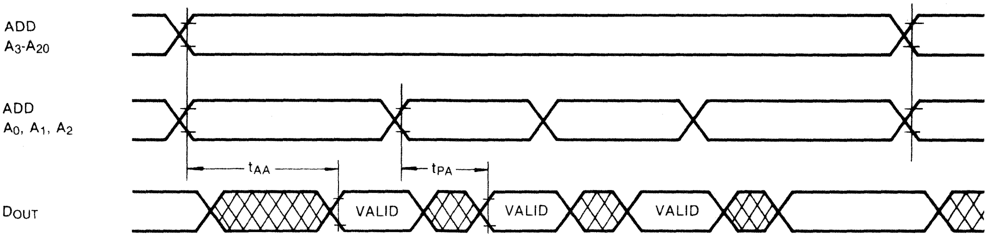
* Page Address: A_0, A_1, A_2

TIMING DIAGRAM

READ



PAGE READ

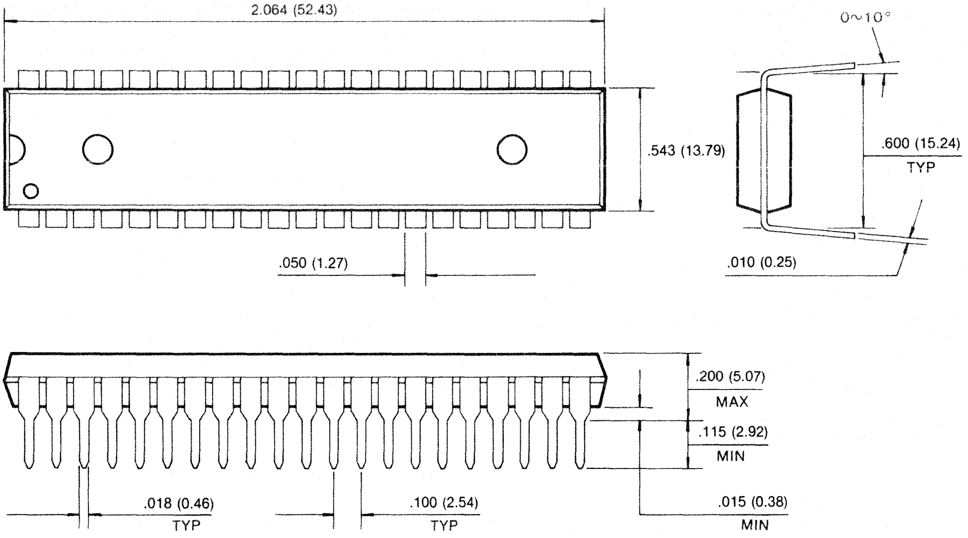


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C32100)

Unit: Inches (mm)

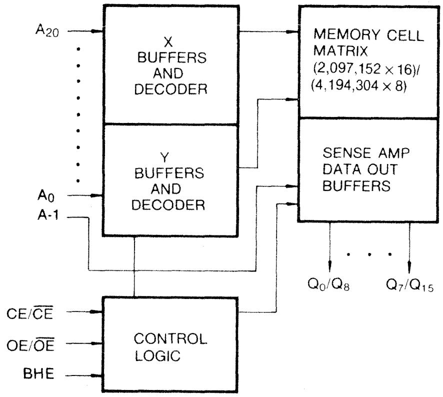


32M-Bit (4M × 8/2M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 × 8 (byte mode)
  2,097,152 × 16 (word mode)
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin, 600 mil, plastic SOP**

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

GENERAL DESCRIPTION

The KM23C32100G is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 × 8 bit (byte mode) or as 2,097,152 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

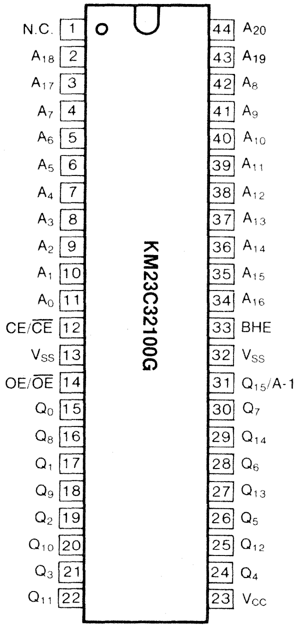
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{20} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32100G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE}=\overline{OE}=V_{IL}$, all output open	f = 6.7MHz	—	100	mA
	I_{CC2}		f = 1.0MHz	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

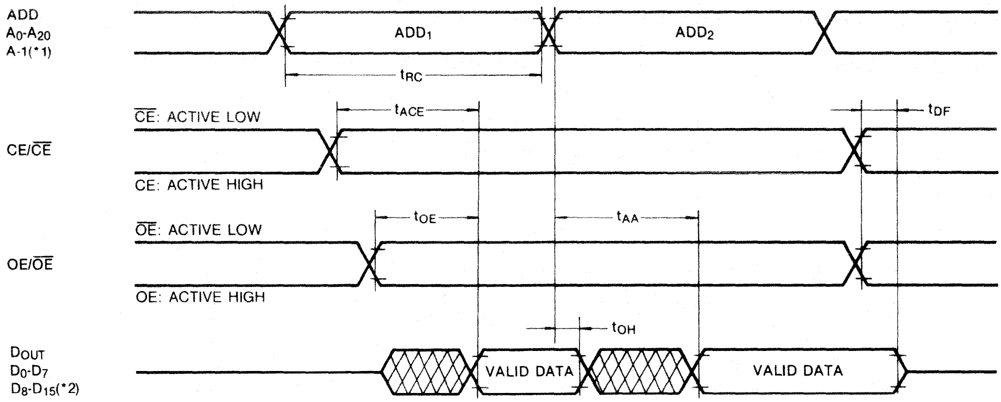
READ CYCLE

Parameter	Symbol	KM23C32100G-15		KM23C32100G-20		KM23C32100G-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

* Page Address: A_0, A_1, A_2

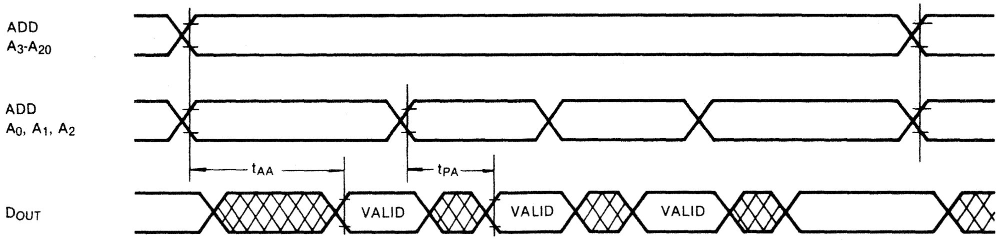
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE$=V_{IL}$)
(*2) Word Mode only. (BHE$=V_{IH}$)

PAGE READ

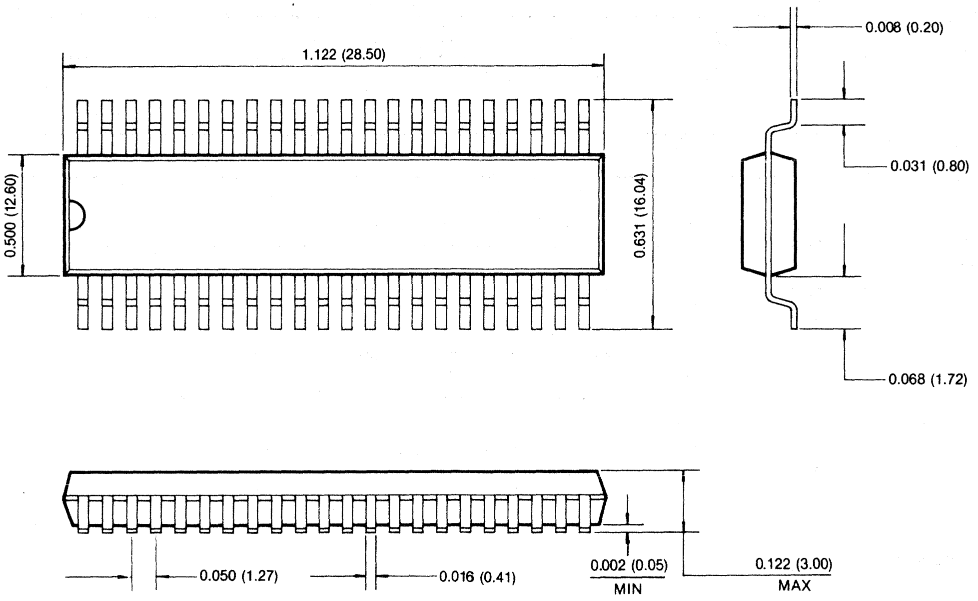


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

44 LEAD SMALL OUTLINE PACKAGE (KM23C32100G)

Unit: Inches (mm)



PRELIMINARY

KM23C32100FP CMOS MASK ROM

32M-Bit (4M × 8/2M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 × 8 (byte mode)
  2,097,152 × 16 (word mode)
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 64-pin QFP (JEDEC standard)**

GENERAL DESCRIPTION

The KM23C32100FP is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 × 8 bit (byte mode) or as 2,097,152 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

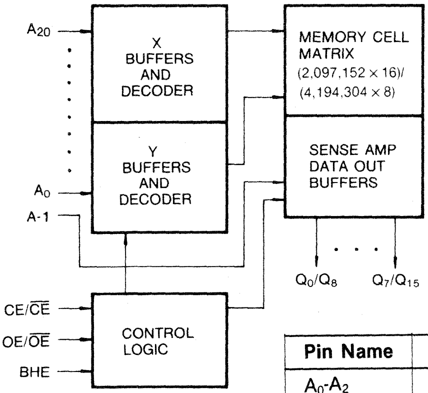
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{20} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

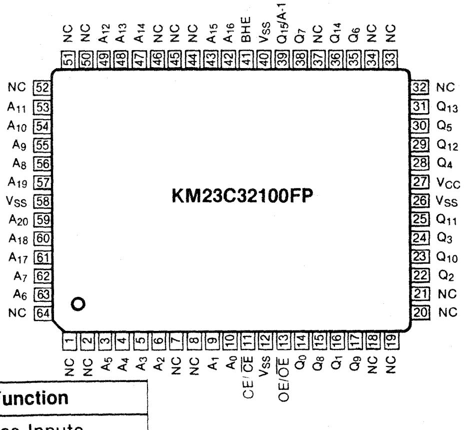
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32100FP is packaged in a 64-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, all output open	f = 6.7MHz	—	100	mA
	I_{CC2}		f = 1.0MHz	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open		—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}			−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		—	0.4	V

CAPACITANCE ($T_a = 25$°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

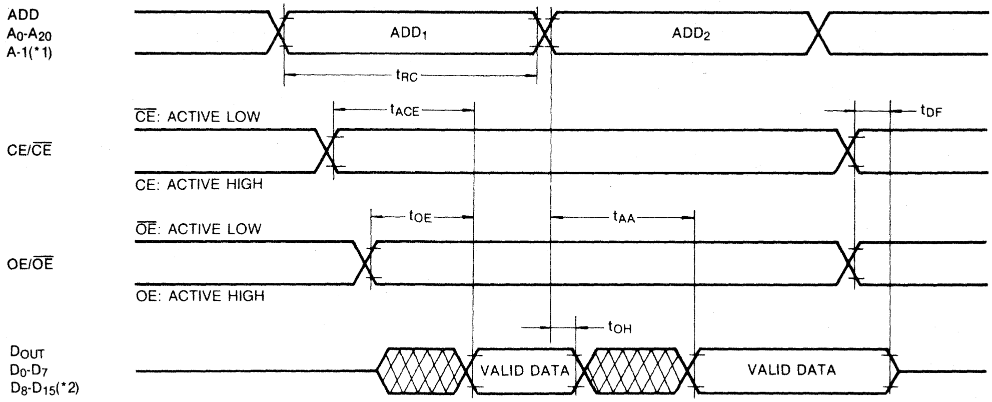
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C32100FP-15		KM23C32100FP-20		KM23C32100FP-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

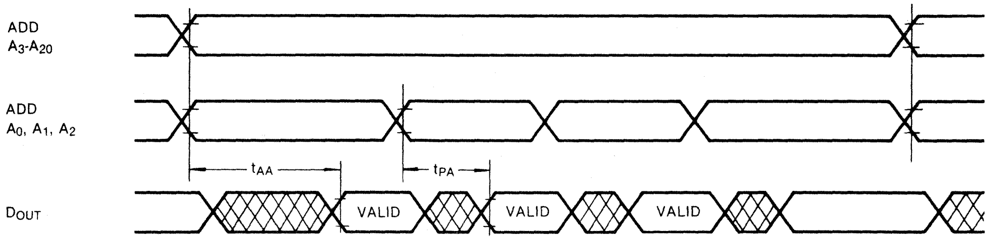
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

PAGE READ

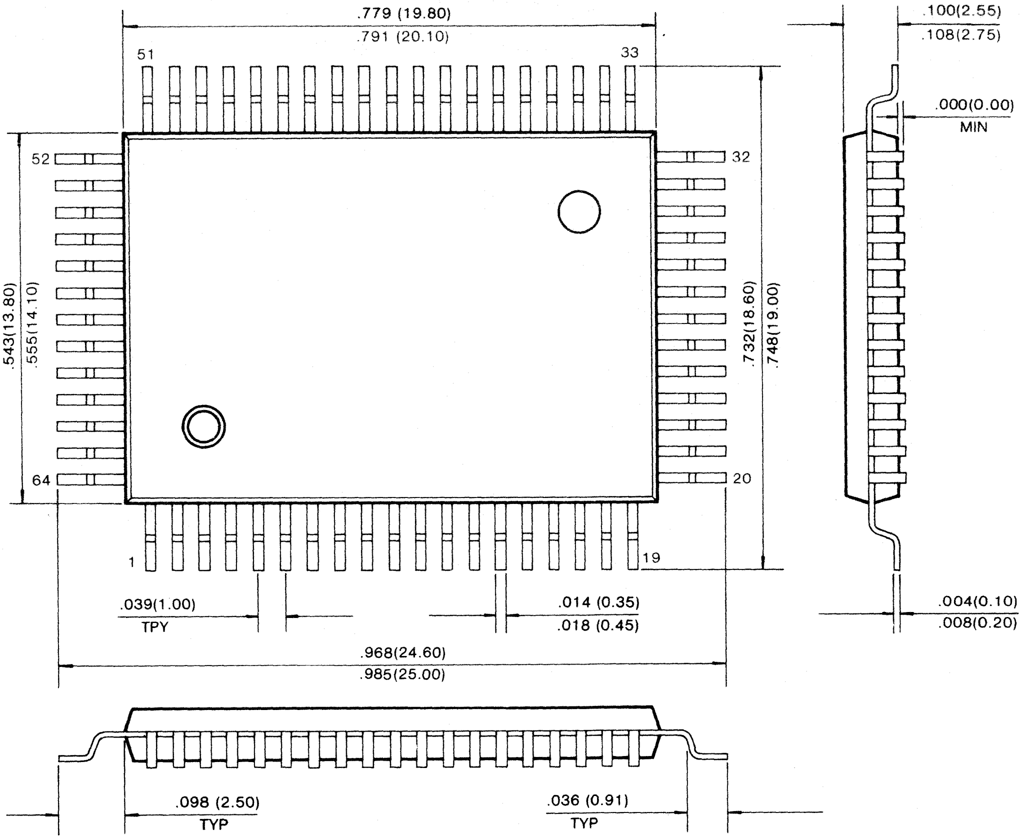


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

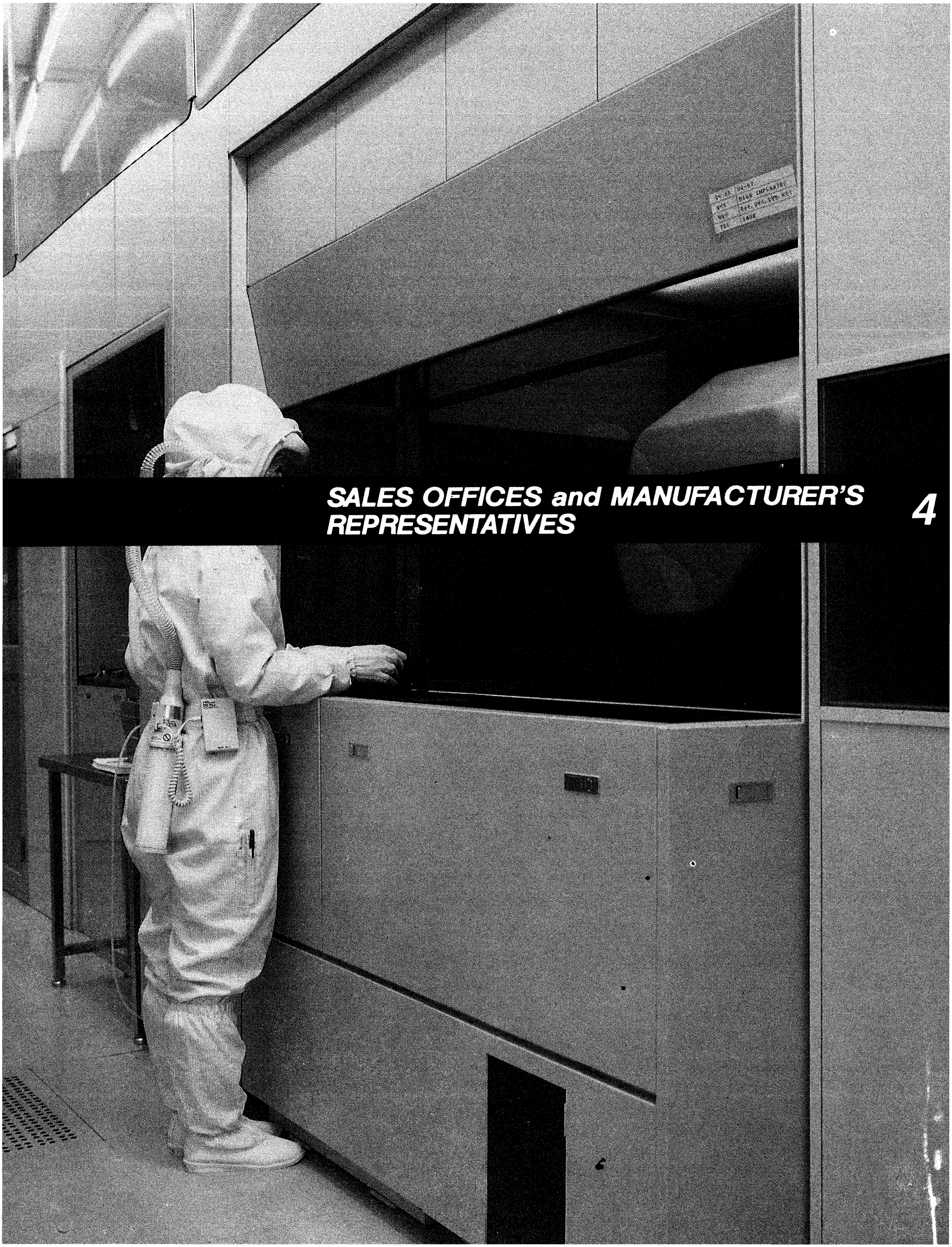
PACKAGE DIMENSIONS

64 LEAD QUADFLAT PACKAGE (KM23C32100FP)

Unit: Inches (mm)



NOTES



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